

ESCHER-Y1 REV-A2

Layout-----ESCHER-H1 REV-A2B2

ES66x8 + SANYO DV34 PICKUP + OUTPUT

Background

This DVD design is based on ESS Vibratio-II ES66x8 single chip DVD mpeg and servo processor. The ES66x8 is built upon ESS proven Programmable Multimedia Processor architecture with integrated servo DSP. A complete DVD design using ES6603 RF-Amp can support all major popular optical pickup heads. With ES66x8 unity memory architecture, the whole system memory is reduced to a minimum. ES66x8 provides the best price performance DVD solution in the industry.

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System Clock Requirement

ES66x8 require a 27MHz clock to operate. This 27MHz can either be generated externally and feed into pin 3 and pin 4 or thru a 27MHz crystal attached to pin 2 and 3. This 27MHz will be used for all video processing reference. In addition, internal multiplier will generate a much higher operating frequency for the internal RISC+DSP code to operate. Audio clock is generated from ES66x8 by its internal PLL circuitry.

SDRAM Usage

ES66x8 support the use of higher density 4Mx16 SDRAM. A single of 4Mx16 SDRAM is sufficient for the whole system to operate.

System Configuration

CHIP	FUNCTION
ES66x8	Single chip processor that handles all system control, DVD decoding and servo control.
64MBIT SDRAM	Data storage and frame buffer
8MBIT EPROM/FLASH	Program storage
24C01 SERIAL EE	System setup configuration storage
WM8706	2-Channel AudioDAC
WM8746	6-Channel AudioDAC
WM8739	2-Channel AudioADC

LCS#	FUNCTION
LCS0#	SPARE
LCS1#	74HCT374 (U16) I/O EXPAND CONTROL
LCS2#	ROM EMULATOR
LCS3#	ROM/FLASH

AUX	FUNCTION
AUX0	I2C DATA
AUX1	I2C CLOCK
AUX2	MICMUTE / HSYNC
AUX3	SCARTCTL / VSYNC
AUX4	IR
AUX5	VFD DATA
AUX6	VFD CS
AUX7	VFD CLK

EAUX	FUNCTION
EAUX00	AUDIODAC MD
EAUX01	AUDIODAC MC
EAUX02	AUDIODAC ML
EAUX03	AUDIODAC CSB#

XGPIO	FUNCTION
XGPIO4	MOCTL / RS232 DET
XGPIO5	CD.DVDC
XGPIO6	OUTSW
XGPIO7	CLOSE
XGPIO8	HOMESW
XGPIO9	INSW

Revision History

Rev-A1

1. Base on Escher-H1 Rev-A4 change pickup from HITACHI HOP1200 to SANYO DV34.

Rev-A2

1. Add pull low resistor on TSD2.
2. Change R92 from 1K to OPEN.
3. Change UJAC to PB change UJAC to PR.

TITLE (標題) ES-6628 DECODE BOARD		DATE / 日期
MODEL (模型) 3003 AMP	USER (用戶)	Y1-2003
REV (版次) B	DR. (工程師) / 工程師	1/7/02
	CRE. (制圖) / 制圖	
	REV. (校對) / 校對	
	REF. (圖內) / 圖內	

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