

D51E5TA7601

Driver IC for 260K-color display on HVGA a-Si TFT

Ver 0.6

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1. Overview

The D51E5TA7601 is a single-chip controller driver LSI for a-Si TFT liquid crystal display of 262,144 colors, with integrated DDRAM for graphics data of 320RGB x 480 dots at maximum, a gate driver, source driver and a power supply circuit.

The D51E5TA7601 supports 18-/16-/9-/8-bit parallel interfaces, 18-/16-bit Serial Peripheral Interface (SPI) and 18-/16-/6-bit RGB interface for motion picture display. The motion picture area can be specified by Window Addressing Function.

The D51E5TA7601 incorporates step-up circuits for generating voltages for driving a TFT LCD and a voltage follower circuits and also supports a function to display images in 8 colors and standby mode for low power consumptions.

The D51E5TA7601 supports Backlight control function with image processing. So, phone-set power consumption could be saved.

The D51E5TA7601 is suitable for any medium or small portable mobile solution required long-term driving capabilities such as mobile TV phones, digital cellular phones, and small PDAs.

2. Features

Overalls

- Single-chip solution to drive an amorphous-silicon TFT panel.
- 320-RGB x 480-dot resolution, 960ch Source driver / 480ch Gate driver

Color Depth

- 262,144 / 65,536 colors can be displayed
- 8 colors can be displayed to save power consumption

Host Interfaces

- 18-/16-/9-/8-bit parallel interfaces
- 18-/16- bit serial peripheral interface (SPI)
- 18-/16-/6-bit RGB interfaces for motion picture display
- VSYNC interface (system interface + VSYNC)

Graphic Operations & Display Direction Control

- Window-Addressing Function to display motion picture independent of still image display
- Image mirroring horizontally & vertically
- Source Output Direction Control (Horizontal Control)
- Gate Scan Direction Control (Vertical Control)
- Gate Scan Start Line Control

Image Quality Improvement Function

- Separated Gamma Control
- 1-line Inversion with mixed Inversion
- VCOM tuning function via user calibration with NVM cells

Low-power operations are supported

- Power-save functions (standby mode, 8-color display mode)
- Partial display (up to two separated screens) in any horizontal position
- A voltage follower circuits for stepping up a liquid crystal drive voltage up to 7 times
- Back Light Control Function with SMLC (Smart Mobile Luminance Control)

Two kinds of power-up sequence are supported

- Automatic power-up sequence
- Manual power-up sequence

Internal power supply circuit

- Step-up circuit : from 4 to 7 times positive-polarity, 3 to 5 times negative-polarity
- Adjustment of VCOM amplitude; internal 247(max) level potentiometer

Operating voltage

◆ Apply voltage

- IOVCI to VSS = 1.65 to 3.3V logic interface level
- VCI to VSSA = 2.5 to 3.3V power supply voltage

◆ Generation voltage

- For the source driver : AVDD to VSSA = 3.5 to 5.5V (power supply for LCD drive circuits)
GVDD to VSSA = 3.0 to 5.0V (reference voltage for grayscale generator)
- For the gate level shifter : VGH to VSSA = 8.75 to 19.25V , VGL to VSSA = -13.25 to -5.25V
VGH to VGL = 14.0V to 27V
- For the step-up circuit : VCI1 to VSSA = 1.7 to 3.0V
- For the TFT-LCD counter electrode : VCOMH to VSSA = 3.0 to 5.0V
VCOML to VSSA = -VCI1 + 0.5V to VSS
VCOM amplitude (max) = 6.0V

Package Type

- COG type only.

3. Block Diagram

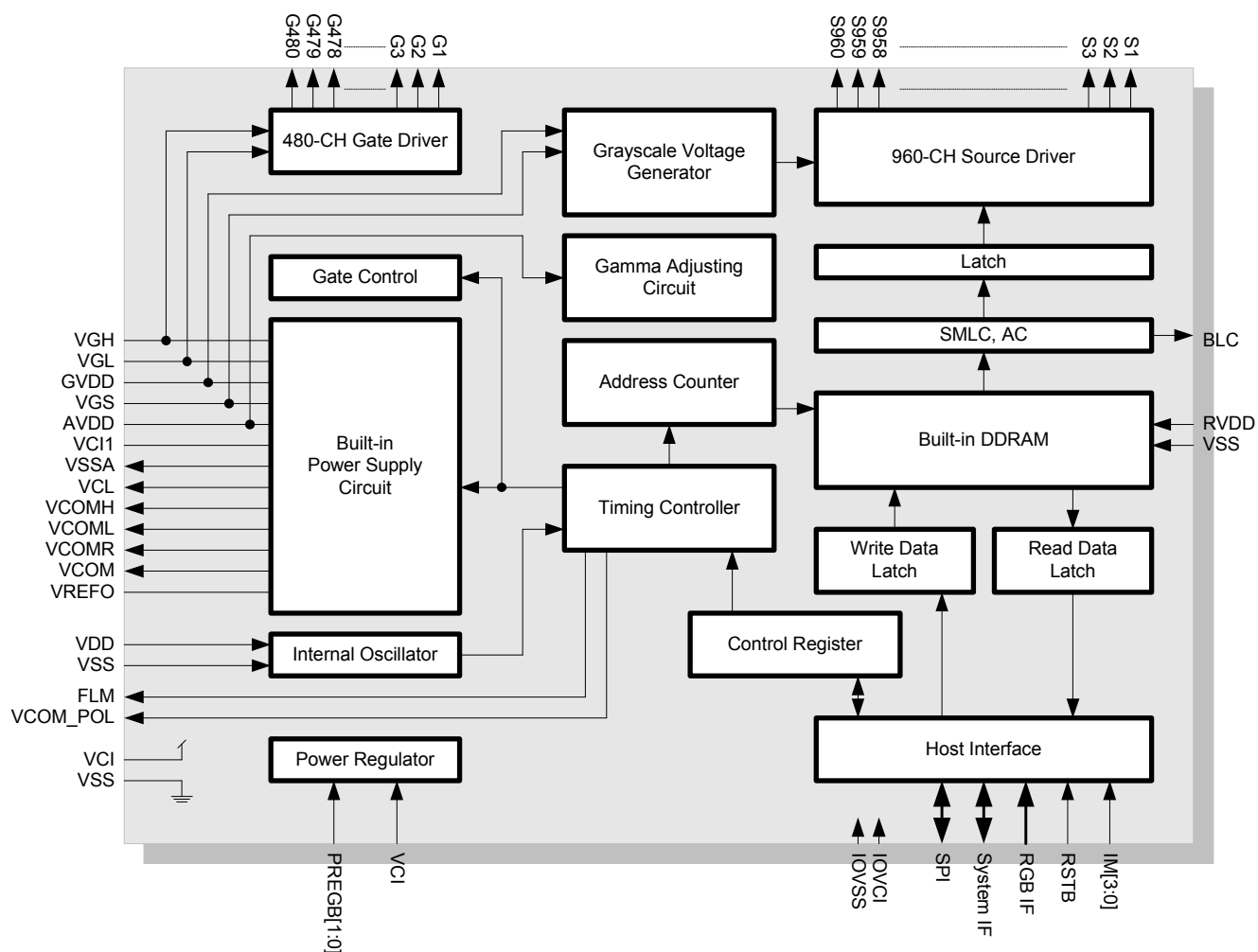


Figure 3-1 : Block Diagram of D51E5TA7601

4. Bump Configuration

4.1. Outline

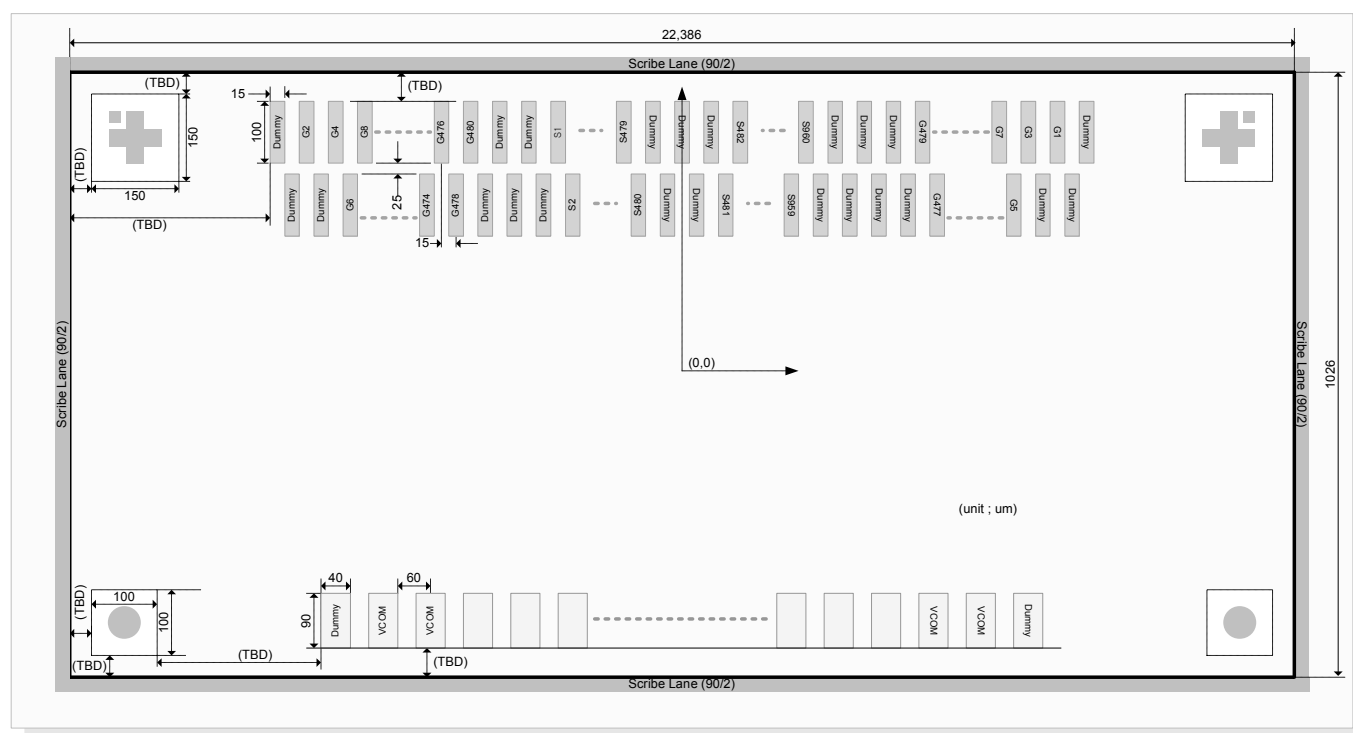


Figure 4-1 : Bump Placement

4.2. Bump Size & Chip Size

Table 4-1 : Chip Size & Bump Size

Items	Category	Size (unit : um)		Remark
		X	Y	
Chip Size	-	22,386	1,026	Without Scribe Lane
Bump Size	Input	40	90	Pitch ; 70
	Output	15	100	Pitch ; 15
Bump Height	All	14 ± 2		

[NOTE] Wafer thickness ; over 300um

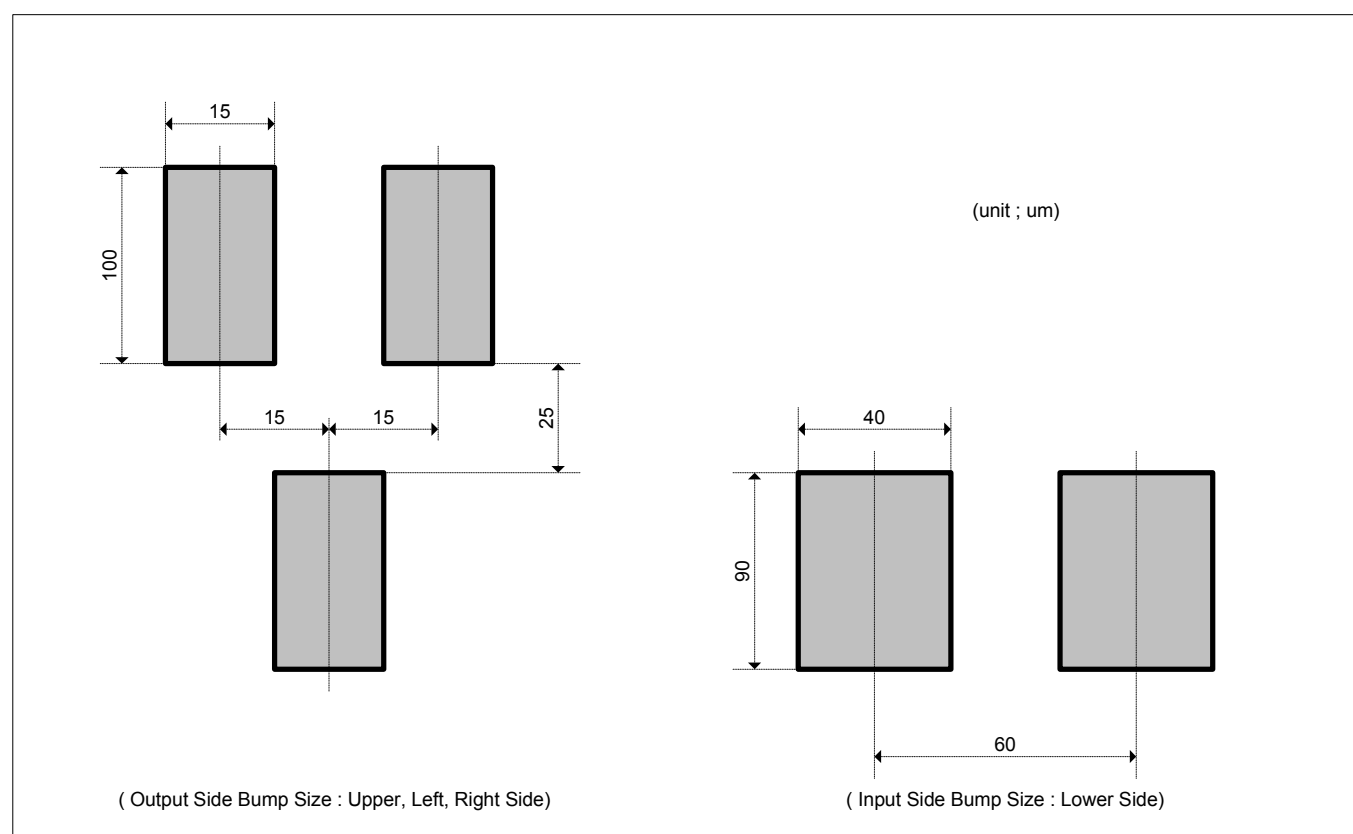


Figure 4-2 : Bump Size

4.3. Alignment Key Dimension

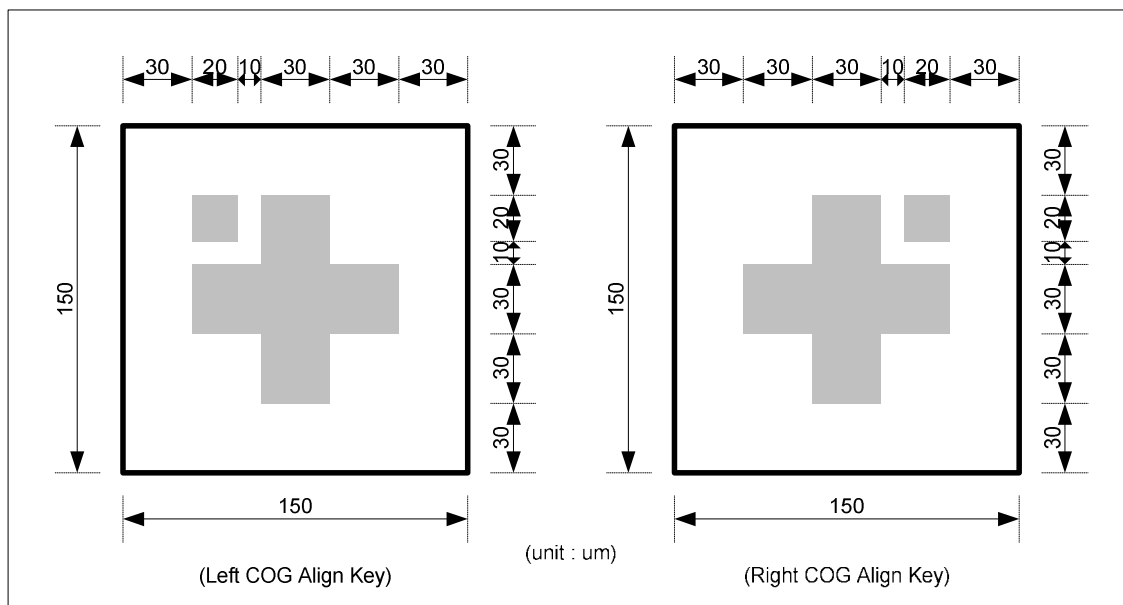


Figure 4-3 : Alignment Key-1 Dimension

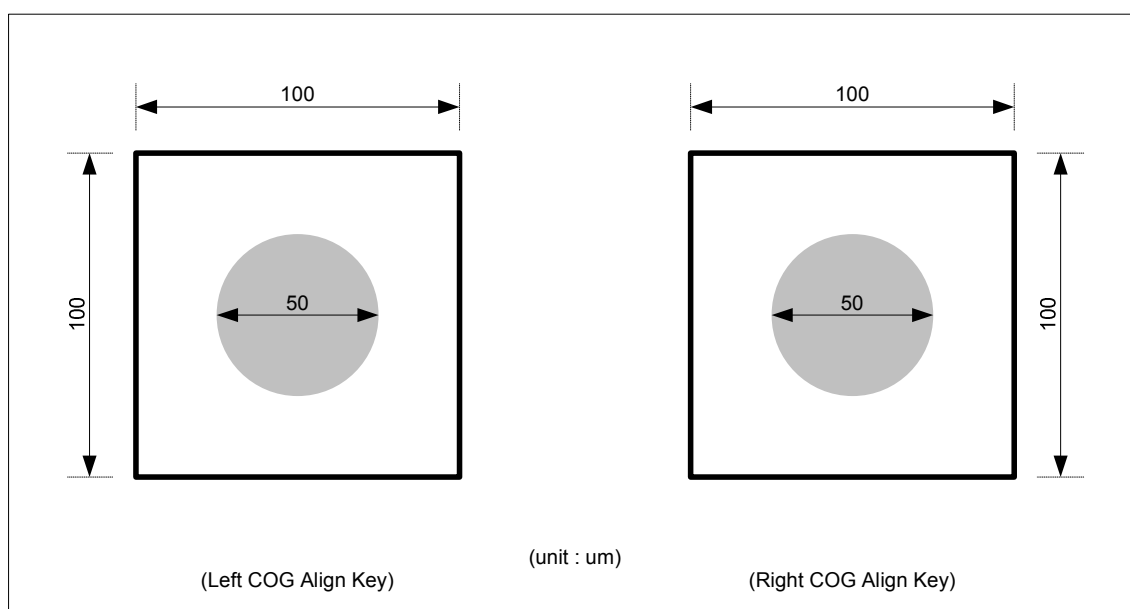


Figure 4-4 : Alignment Key-2 Dimension

4.4. Bump Coordinates

Table 4-2 : Bump Coordinates of TA7601

No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)
1	KEY_2 LEFT	-11135	-455	51	C12P	-7525	-456	101	GMON	-4025	-456
2	DUMMY0	-10955	-456	52	C12P	-7455	-456	102	VGS	-3955	-456
3	VCOM	-10885	-456	53	C12P	-7385	-456	103	VGS	-3885	-456
4	VCOM	-10815	-456	54	C11M	-7315	-456	104	VSSA	-3815	-456
5	VCOM	-10745	-456	55	C11M	-7245	-456	105	VSSA	-3745	-456
6	VCOM	-10675	-456	56	C11M	-7175	-456	106	VSSA	-3675	-456
7	DUMMY1	-10605	-456	57	C11M	-7105	-456	107	VSSA	-3605	-456
8	VCOML	-10535	-456	58	C11M	-7035	-456	108	VSSA	-3535	-456
9	VCOML	-10465	-456	59	C11M	-6965	-456	109	VSSA	-3465	-456
10	VCOML	-10395	-456	60	C11M	-6895	-456	110	VSSA	-3395	-456
11	VCOML	-10325	-456	61	C11M	-6825	-456	111	VSSA	-3325	-456
12	VCOML	-10255	-456	62	C11P	-6755	-456	112	VSSA	-3255	-456
13	VCOML	-10185	-456	63	C11P	-6685	-456	113	VSSA	-3185	-456
14	VCOML	-10115	-456	64	C11P	-6615	-456	114	VSSA	-3115	-456
15	VCOML	-10045	-456	65	C11P	-6545	-456	115	VSS	-3045	-456
16	VCOML	-9975	-456	66	C11P	-6475	-456	116	VSS	-2975	-456
17	VCOML	-9905	-456	67	C11P	-6405	-456	117	VSS	-2905	-456
18	VCOMH	-9835	-456	68	C11P	-6335	-456	118	VSS	-2835	-456
19	VCOMH	-9765	-456	69	C11P	-6265	-456	119	VSS	-2765	-456
20	VCOMH	-9695	-456	70	AVDD	-6195	-456	120	VSS	-2695	-456
21	VCOMH	-9625	-456	71	AVDD	-6125	-456	121	RVDD	-2625	-456
22	VCOMH	-9555	-456	72	AVDD	-6055	-456	122	RVDD	-2555	-456
23	VCOMH	-9485	-456	73	AVDD	-5985	-456	123	RVDD	-2485	-456
24	VCOMH	-9415	-456	74	AVDD	-5915	-456	124	RVDD	-2415	-456
25	VCOMH	-9345	-456	75	AVDD	-5845	-456	125	RVDD	-2345	-456
26	VCOMH	-9275	-456	76	AVDD	-5775	-456	126	VDD	-2275	-456
27	VCOMH	-9205	-456	77	VCI1	-5705	-456	127	VDD	-2205	-456
28	VCOMH	-9135	-456	78	VCI1	-5635	-456	128	VDD	-2135	-456
29	VCOMR	-9065	-456	79	VCI1	-5565	-456	129	VDD	-2065	-456
30	VCOMR	-8995	-456	80	VCI1	-5495	-456	130	VDD	-1995	-456
31	GVDD	-8925	-456	81	VCI1	-5425	-456	131	IOVSS	-1925	-456
32	GVDD	-8855	-456	82	VCI	-5355	-456	132	IOVSS	-1855	-456
33	GVDD	-8785	-456	83	VCI	-5285	-456	133	IOVSS	-1785	-456
34	GVDD	-8715	-456	84	VCI	-5215	-456	134	PREGB1	-1715	-456
35	GVDD	-8645	-456	85	VCI	-5145	-456	135	PREGB0	-1645	-456
36	GVDD	-8575	-456	86	VCI	-5075	-456	136	IOVCI	-1575	-456
37	DUMMY2	-8505	-456	87	VCI	-5005	-456	137	IOVCI	-1505	-456
38	C12M	-8435	-456	88	VCI	-4935	-456	138	IOVCI	-1435	-456
39	C12M	-8365	-456	89	VCI	-4865	-456	139	IOVCI	-1365	-456
40	C12M	-8295	-456	90	VCI	-4795	-456	140	CSB	-1295	-456
41	C12M	-8225	-456	91	VCI	-4725	-456	141	RWB_RDB	-1225	-456
42	C12M	-8155	-456	92	VCI	-4655	-456	142	RS	-1155	-456
43	C12M	-8085	-456	93	VCI	-4585	-456	143	E_WRB	-1085	-456
44	C12M	-8015	-456	94	VCI	-4515	-456	144	VSYN	-1015	-456
45	C12M	-7945	-456	95	VCI	-4445	-456	145	HSYN	-945	-456
46	C12P	-7875	-456	96	VCI	-4375	-456	146	DOTCLK	-875	-456
47	C12P	-7805	-456	97	VCI	-4305	-456	147	ENABLE	-805	-456
48	C12P	-7735	-456	98	VCI	-4235	-456	148	SDO	-735	-456
49	C12P	-7665	-456	99	VREFO	-4165	-456	149	SDI	-665	-456
50	C12P	-7595	-456	100	VREFO	-4095	-456	150	SCL	-595	-456

No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)
151	RSTB	-525	-456	201	OTPV	2975	-456	251	VGL	6475	-456
152	IOVSS	-455	-456	202	OTPV	3045	-456	252	VGL	6545	-456
153	DUMMY3	-385	-456	203	OTPV	3115	-456	253	VGL	6615	-456
154	DUMMY4	-315	-456	204	OTPV	3185	-456	254	VGL	6685	-456
155	DUMMY5	-245	-456	205	C31P	3255	-456	255	VGL	6755	-456
156	DUMMY6	-175	-456	206	C31P	3325	-456	256	VGL	6825	-456
157	DUMMY7	-105	-456	207	C31P	3395	-456	257	C22M	6895	-456
158	DUMMY8	-35	-456	208	C31P	3465	-456	258	C22M	6965	-456
159	IOVSS	35	-456	209	C31P	3535	-456	259	C22M	7035	-456
160	DB17	105	-456	210	C31P	3605	-456	260	C22M	7105	-456
161	DB16	175	-456	211	C31M	3675	-456	261	C22M	7175	-456
162	DB15	245	-456	212	C31M	3745	-456	262	C22M	7245	-456
163	DB14	315	-456	213	C31M	3815	-456	263	C22M	7315	-456
164	DB13	385	-456	214	C31M	3885	-456	264	C22M	7385	-456
165	DB12	455	-456	215	C31M	3955	-456	265	C22M	7455	-456
166	DB11	525	-456	216	C31M	4025	-456	266	C22M	7525	-456
167	DB10	595	-456	217	VCL	4095	-456	267	C22M	7595	-456
168	DB9	665	-456	218	VCL	4165	-456	268	C22M	7665	-456
169	DB8	735	-456	219	VCL	4235	-456	269	C22M	7735	-456
170	DB7	805	-456	220	VCL	4305	-456	270	C22M	7805	-456
171	DB6	875	-456	221	VCL	4375	-456	271	C22P	7875	-456
172	DB5	945	-456	222	VCL	4445	-456	272	C22P	7945	-456
173	DB4	1015	-456	223	PGND	4515	-456	273	C22P	8015	-456
174	DB3	1085	-456	224	PGND	4585	-456	274	C22P	8085	-456
175	DB2	1155	-456	225	PGND	4655	-456	275	C22P	8155	-456
176	DB1	1225	-456	226	PGND	4725	-456	276	C22P	8225	-456
177	DB0	1295	-456	227	PGND	4795	-456	277	C22P	8295	-456
178	IOVCI	1365	-456	228	PGND	4865	-456	278	C22P	8365	-456
179	SPI3	1435	-456	229	PGND	4935	-456	279	C22P	8435	-456
180	IM3	1505	-456	230	PGND	5005	-456	280	C22P	8505	-456
181	IM2	1575	-456	231	PGND	5075	-456	281	C22P	8575	-456
182	IM1	1645	-456	232	PGND	5145	-456	282	C22P	8645	-456
183	IM0	1715	-456	233	VGH	5215	-456	283	C22P	8715	-456
184	TEST_MODE3	1785	-456	234	VGH	5285	-456	284	C22P	8785	-456
185	TEST_MODE2	1855	-456	235	VGH	5355	-456	285	C21M	8855	-456
186	TEST_MODE1	1925	-456	236	VGH	5425	-456	286	C21M	8925	-456
187	TEST_MODE0	1995	-456	237	VGH	5495	-456	287	C21M	8995	-456
188	IOVSS	2065	-456	238	VGH	5565	-456	288	C21M	9065	-456
189	TEST_IN4	2135	-456	239	VGH	5635	-456	289	C21M	9135	-456
190	TEST_IN3	2205	-456	240	VGH	5705	-456	290	C21M	9205	-456
191	TEST_IN2	2275	-456	241	VGH	5775	-456	291	C21M	9275	-456
192	TEST_IN1	2345	-456	242	VGH	5845	-456	292	C21M	9345	-456
193	TEST_IN0	2415	-456	243	VGH	5915	-456	293	C21M	9415	-456
194	TEST_OUT3	2485	-456	244	VGH	5985	-456	294	C21M	9485	-456
195	TEST_OUT2	2555	-456	245	VGL	6055	-456	295	C21M	9555	-456
196	TEST_OUT1	2625	-456	246	VGL	6125	-456	296	C21M	9625	-456
197	TEST_OUT0	2695	-456	247	VGL	6195	-456	297	C12P	9695	-456
198	FLM	2765	-456	248	VGL	6265	-456	298	C21P	9765	-456
199	BLC	2835	-456	249	VGL	6335	-456	299	C21P	9835	-456
200	VCOM_POL	2905	-456	250	VGL	6405	-456	300	C21P	9905	-456

No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)
301	C21P	9975	-456	351	G61	10485	328	401	G161	9735	328
302	C21P	10045	-456	352	G63	10470	453	402	G163	9720	453
303	C21P	10115	-456	353	G65	10455	328	403	G165	9705	328
304	C21P	10185	-456	354	G67	10440	453	404	G167	9690	453
305	C21P	10255	-456	355	G69	10425	328	405	G169	9675	328
306	C21P	10325	-456	356	G71	10410	453	406	G171	9660	453
307	C21P	10395	-456	357	G73	10395	328	407	G173	9645	328
308	C21P	10465	-456	358	G75	10380	453	408	G175	9630	453
309	CONT1	10535	-456	359	G77	10365	328	409	G177	9615	328
310	CONT0	10605	-456	360	G79	10350	453	410	G179	9600	453
311	VCOM	10675	-456	361	G81	10335	328	411	G181	9585	328
312	VCOM	10745	-456	362	G83	10320	453	412	G183	9570	453
313	VCOM	10815	-456	363	G85	10305	328	413	G185	9555	328
314	VCOM	10885	-456	364	G87	10290	453	414	G187	9540	453
315	DUMMY9	10955	-456	365	G89	10275	328	415	G189	9525	328
316	KEY_2 RIGHT	11135	-455	366	G91	10260	453	416	G191	9510	453
317	KEY_1 RIGHT	11110	430	367	G93	10245	328	417	G193	9495	328
318	DUMMY10	10980	453	368	G95	10230	453	418	G195	9480	453
319	DUMMY11	10965	328	369	G97	10215	328	419	G197	9465	328
320	G1	10950	453	370	G99	10200	453	420	G199	9450	453
321	DUMMY12	10935	328	371	G101	10185	328	421	G201	9435	328
322	G3	10920	453	372	G103	10170	453	422	G203	9420	453
323	G5	10905	328	373	G105	10155	328	423	G205	9405	328
324	G7	10890	453	374	G107	10140	453	424	G207	9390	453
325	G9	10875	328	375	G109	10125	328	425	G209	9375	328
326	G11	10860	453	376	G111	10110	453	426	G211	9360	453
327	G13	10845	328	377	G113	10095	328	427	G213	9345	328
328	G15	10830	453	378	G115	10080	453	428	G215	9330	453
329	G17	10815	328	379	G117	10065	328	429	G217	9315	328
330	G19	10800	453	380	G119	10050	453	430	G219	9300	453
331	G21	10785	328	381	G121	10035	328	431	G221	9285	328
332	G23	10770	453	382	G123	10020	453	432	G223	9270	453
333	G25	10755	328	383	G125	10005	328	433	G225	9255	328
334	G27	10740	453	384	G127	9990	453	434	G227	9240	453
335	G29	10725	328	385	G129	9975	328	435	G229	9225	328
336	G31	10710	453	386	G131	9960	453	436	G231	9210	453
337	G33	10695	328	387	G133	9945	328	437	G233	9195	328
338	G35	10680	453	388	G135	9930	453	438	G235	9180	453
339	G37	10665	328	389	G137	9915	328	439	G237	9165	328
340	G39	10650	453	390	G139	9900	453	440	G239	9150	453
341	G41	10635	328	391	G141	9885	328	441	G241	9135	328
342	G43	10620	453	392	G143	9870	453	442	G243	9120	453
343	G45	10605	328	393	G145	9855	328	443	G245	9105	328
344	G47	10590	453	394	G147	9840	453	444	G247	9090	453
345	G49	10575	328	395	G149	9825	328	445	G249	9075	328
346	G51	10560	453	396	G151	9810	453	446	G251	9060	453
347	G53	10545	328	397	G153	9795	328	447	G253	9045	328
348	G55	10530	453	398	G155	9780	453	448	G255	9030	453
349	G57	10515	328	399	G157	9765	328	449	G257	9015	328
350	G59	10500	453	400	G159	9750	453	450	G259	9000	453

No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)
451	G261	8985	328	501	G361	8235	328	551	G461	7485	328
452	G263	8970	453	502	G363	8220	453	552	G463	7470	453
453	G265	8955	328	503	G365	8205	328	553	G465	7455	328
454	G267	8940	453	504	G367	8190	453	554	G467	7440	453
455	G269	8925	328	505	G369	8175	328	555	G469	7425	328
456	G271	8910	453	506	G371	8160	453	556	G471	7410	453
457	G273	8895	328	507	G373	8145	328	557	G473	7395	328
458	G275	8880	453	508	G375	8130	453	558	G475	7380	453
459	G277	8865	328	509	G377	8115	328	559	G477	7365	328
460	G279	8850	453	510	G379	8100	453	560	G479	7350	453
461	G281	8835	328	511	G381	8085	328	561	DUMMY13	7335	328
462	G283	8820	453	512	G383	8070	453	562	DUMMY14	7320	453
463	G285	8805	328	513	G385	8055	328	563	DUMMY15	7305	328
464	G287	8790	453	514	G387	8040	453	564	DUMMY16	7290	453
465	G289	8775	328	515	G389	8025	328	565	DUMMY17	7275	328
466	G291	8760	453	516	G391	8010	453	566	DUMMY18	7260	453
467	G293	8745	328	517	G393	7995	328	567	DUMMY19	7245	328
468	G295	8730	453	518	G395	7980	453	568	S960	7230	453
469	G297	8715	328	519	G397	7965	328	569	S959	7215	328
470	G299	8700	453	520	G399	7950	453	570	S958	7200	453
471	G301	8685	328	521	G401	7935	328	571	S957	7185	328
472	G303	8670	453	522	G403	7920	453	572	S956	7170	453
473	G305	8655	328	523	G405	7905	328	573	S955	7155	328
474	G307	8640	453	524	G407	7890	453	574	S954	7140	453
475	G309	8625	328	525	G409	7875	328	575	S953	7125	328
476	G311	8610	453	526	G411	7860	453	576	S952	7110	453
477	G313	8595	328	527	G413	7845	328	577	S951	7095	328
478	G315	8580	453	528	G415	7830	453	578	S950	7080	453
479	G317	8565	328	529	G417	7815	328	579	S949	7065	328
480	G319	8550	453	530	G419	7800	453	580	S948	7050	453
481	G321	8535	328	531	G421	7785	328	581	S947	7035	328
482	G323	8520	453	532	G423	7770	453	582	S946	7020	453
483	G325	8505	328	533	G425	7755	328	583	S945	7005	328
484	G327	8490	453	534	G427	7740	453	584	S944	6990	453
485	G329	8475	328	535	G429	7725	328	585	S943	6975	328
486	G331	8460	453	536	G431	7710	453	586	S942	6960	453
487	G333	8445	328	537	G433	7695	328	587	S941	6945	328
488	G335	8430	453	538	G435	7680	453	588	S940	6930	453
489	G337	8415	328	539	G437	7665	328	589	S939	6915	328
490	G339	8400	453	540	G439	7650	453	590	S938	6900	453
491	G341	8385	328	541	G441	7635	328	591	S937	6885	328
492	G343	8370	453	542	G443	7620	453	592	S936	6870	453
493	G345	8355	328	543	G445	7605	328	593	S935	6855	328
494	G347	8340	453	544	G447	7590	453	594	S934	6840	453
495	G349	8325	328	545	G449	7575	328	595	S933	6825	328
496	G351	8310	453	546	G451	7560	453	596	S932	6810	453
497	G353	8295	328	547	G453	7545	328	597	S931	6795	328
498	G355	8280	453	548	G455	7530	453	598	S930	6780	453
499	G357	8265	328	549	G457	7515	328	599	S929	6765	328
500	G359	8250	453	550	G459	7500	453	600	S928	6750	453

No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)
601	S927	6735	328	651	S877	5985	328	701	S827	5235	328
602	S926	6720	453	652	S876	5970	453	702	S826	5220	453
603	S925	6705	328	653	S875	5955	328	703	S825	5205	328
604	S924	6690	453	654	S874	5940	453	704	S824	5190	453
605	S923	6675	328	655	S873	5925	328	705	S823	5175	328
606	S922	6660	453	656	S872	5910	453	706	S822	5160	453
607	S921	6645	328	657	S871	5895	328	707	S821	5145	328
608	S920	6630	453	658	S870	5880	453	708	S820	5130	453
609	S919	6615	328	659	S869	5865	328	709	S819	5115	328
610	S918	6600	453	660	S868	5850	453	710	S818	5100	453
611	S917	6585	328	661	S867	5835	328	711	S817	5085	328
612	S916	6570	453	662	S866	5820	453	712	S816	5070	453
613	S915	6555	328	663	S865	5805	328	713	S815	5055	328
614	S914	6540	453	664	S864	5790	453	714	S814	5040	453
615	S913	6525	328	665	S863	5775	328	715	S813	5025	328
616	S912	6510	453	666	S862	5760	453	716	S812	5010	453
617	S911	6495	328	667	S861	5745	328	717	S811	4995	328
618	S910	6480	453	668	S860	5730	453	718	S810	4980	453
619	S909	6465	328	669	S859	5715	328	719	S809	4965	328
620	S908	6450	453	670	S858	5700	453	720	S808	4950	453
621	S907	6435	328	671	S857	5685	328	721	S807	4935	328
622	S906	6420	453	672	S856	5670	453	722	S806	4920	453
623	S905	6405	328	673	S855	5655	328	723	S805	4905	328
624	S904	6390	453	674	S854	5640	453	724	S804	4890	453
625	S903	6375	328	675	S853	5625	328	725	S803	4875	328
626	S902	6360	453	676	S852	5610	453	726	S802	4860	453
627	S901	6345	328	677	S851	5595	328	727	S801	4845	328
628	S900	6330	453	678	S850	5580	453	728	S800	4830	453
629	S899	6315	328	679	S849	5565	328	729	S799	4815	328
630	S898	6300	453	680	S848	5550	453	730	S798	4800	453
631	S897	6285	328	681	S847	5535	328	731	S797	4785	328
632	S896	6270	453	682	S846	5520	453	732	S796	4770	453
633	S895	6255	328	683	S845	5505	328	733	S795	4755	328
634	S894	6240	453	684	S844	5490	453	734	S794	4740	453
635	S893	6225	328	685	S843	5475	328	735	S793	4725	328
636	S892	6210	453	686	S842	5460	453	736	S792	4710	453
637	S891	6195	328	687	S841	5445	328	737	S791	4695	328
638	S890	6180	453	688	S840	5430	453	738	S790	4680	453
639	S889	6165	328	689	S839	5415	328	739	S789	4665	328
640	S888	6150	453	690	S838	5400	453	740	S788	4650	453
641	S887	6135	328	691	S837	5385	328	741	S787	4635	328
642	S886	6120	453	692	S836	5370	453	742	S786	4620	453
643	S885	6105	328	693	S835	5355	328	743	S785	4605	328
644	S884	6090	453	694	S834	5340	453	744	S784	4590	453
645	S883	6075	328	695	S833	5325	328	745	S783	4575	328
646	S882	6060	453	696	S832	5310	453	746	S782	4560	453
647	S881	6045	328	697	S831	5295	328	747	S781	4545	328
648	S880	6030	453	698	S830	5280	453	748	S780	4530	453
649	S879	6015	328	699	S829	5265	328	749	S779	4515	328
650	S878	6000	453	700	S828	5250	453	750	S778	4500	453

No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)
751	S777	4485	328	801	S727	3735	328	851	S677	2985	328
752	S776	4470	453	802	S726	3720	453	852	S676	2970	453
753	S775	4455	328	803	S725	3705	328	853	S675	2955	328
754	S774	4440	453	804	S724	3690	453	854	S674	2940	453
755	S773	4425	328	805	S723	3675	328	855	S673	2925	328
756	S772	4410	453	806	S722	3660	453	856	S672	2910	453
757	S771	4395	328	807	S721	3645	328	857	S671	2895	328
758	S770	4380	453	808	S720	3630	453	858	S670	2880	453
759	S769	4365	328	809	S719	3615	328	859	S669	2865	328
760	S768	4350	453	810	S718	3600	453	860	S668	2850	453
761	S767	4335	328	811	S717	3585	328	861	S667	2835	328
762	S766	4320	453	812	S716	3570	453	862	S666	2820	453
763	S765	4305	328	813	S715	3555	328	863	S665	2805	328
764	S764	4290	453	814	S714	3540	453	864	S664	2790	453
765	S763	4275	328	815	S713	3525	328	865	S663	2775	328
766	S762	4260	453	816	S712	3510	453	866	S662	2760	453
767	S761	4245	328	817	S711	3495	328	867	S661	2745	328
768	S760	4230	453	818	S710	3480	453	868	S660	2730	453
769	S759	4215	328	819	S709	3465	328	869	S659	2715	328
770	S758	4200	453	820	S708	3450	453	870	S658	2700	453
771	S757	4185	328	821	S707	3435	328	871	S657	2685	328
772	S756	4170	453	822	S706	3420	453	872	S656	2670	453
773	S755	4155	328	823	S705	3405	328	873	S655	2655	328
774	S754	4140	453	824	S704	3390	453	874	S654	2640	453
775	S753	4125	328	825	S703	3375	328	875	S653	2625	328
776	S752	4110	453	826	S702	3360	453	876	S652	2610	453
777	S751	4095	328	827	S701	3345	328	877	S651	2595	328
778	S750	4080	453	828	S700	3330	453	878	S650	2580	453
779	S749	4065	328	829	S699	3315	328	879	S649	2565	328
780	S748	4050	453	830	S698	3300	453	880	S648	2550	453
781	S747	4035	328	831	S697	3285	328	881	S647	2535	328
782	S746	4020	453	832	S696	3270	453	882	S646	2520	453
783	S745	4005	328	833	S695	3255	328	883	S645	2505	328
784	S744	3990	453	834	S694	3240	453	884	S644	2490	453
785	S743	3975	328	835	S693	3225	328	885	S643	2475	328
786	S742	3960	453	836	S692	3210	453	886	S642	2460	453
787	S741	3945	328	837	S691	3195	328	887	S641	2445	328
788	S740	3930	453	838	S690	3180	453	888	S640	2430	453
789	S739	3915	328	839	S689	3165	328	889	S639	2415	328
790	S738	3900	453	840	S688	3150	453	890	S638	2400	453
791	S737	3885	328	841	S687	3135	328	891	S637	2385	328
792	S736	3870	453	842	S686	3120	453	892	S636	2370	453
793	S735	3855	328	843	S685	3105	328	893	S635	2355	328
794	S734	3840	453	844	S684	3090	453	894	S634	2340	453
795	S733	3825	328	845	S683	3075	328	895	S633	2325	328
796	S732	3810	453	846	S682	3060	453	896	S632	2310	453
797	S731	3795	328	847	S681	3045	328	897	S631	2295	328
798	S730	3780	453	848	S680	3030	453	898	S630	2280	453
799	S729	3765	328	849	S679	3015	328	899	S629	2265	328
800	S728	3750	453	850	S678	3000	453	900	S628	2250	453

No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)
901	S627	2235	328	951	S577	1485	328	1001	S527	735	328
902	S626	2220	453	952	S576	1470	453	1002	S526	720	453
903	S625	2205	328	953	S575	1455	328	1003	S525	705	328
904	S624	2190	453	954	S574	1440	453	1004	S524	690	453
905	S623	2175	328	955	S573	1425	328	1005	S523	675	328
906	S622	2160	453	956	S572	1410	453	1006	S522	660	453
907	S621	2145	328	957	S571	1395	328	1007	S521	645	328
908	S620	2130	453	958	S570	1380	453	1008	S520	630	453
909	S619	2115	328	959	S569	1365	328	1009	S519	615	328
910	S618	2100	453	960	S568	1350	453	1010	S518	600	453
911	S617	2085	328	961	S567	1335	328	1011	S517	585	328
912	S616	2070	453	962	S566	1320	453	1012	S516	570	453
913	S615	2055	328	963	S565	1305	328	1013	S515	555	328
914	S614	2040	453	964	S564	1290	453	1014	S514	540	453
915	S613	2025	328	965	S563	1275	328	1015	S513	525	328
916	S612	2010	453	966	S562	1260	453	1016	S512	510	453
917	S611	1995	328	967	S561	1245	328	1017	S511	495	328
918	S610	1980	453	968	S560	1230	453	1018	S510	480	453
919	S609	1965	328	969	S559	1215	328	1019	S509	465	328
920	S608	1950	453	970	S558	1200	453	1020	S508	450	453
921	S607	1935	328	971	S557	1185	328	1021	S507	435	328
922	S606	1920	453	972	S556	1170	453	1022	S506	420	453
923	S605	1905	328	973	S555	1155	328	1023	S505	405	328
924	S604	1890	453	974	S554	1140	453	1024	S504	390	453
925	S603	1875	328	975	S553	1125	328	1025	S503	375	328
926	S602	1860	453	976	S552	1110	453	1026	S502	360	453
927	S601	1845	328	977	S551	1095	328	1027	S501	345	328
928	S600	1830	453	978	S550	1080	453	1028	S500	330	453
929	S599	1815	328	979	S549	1065	328	1029	S499	315	328
930	S598	1800	453	980	S548	1050	453	1030	S498	300	453
931	S597	1785	328	981	S547	1035	328	1031	S497	285	328
932	S596	1770	453	982	S546	1020	453	1032	S496	270	453
933	S595	1755	328	983	S545	1005	328	1033	S495	255	328
934	S594	1740	453	984	S544	990	453	1034	S494	240	453
935	S593	1725	328	985	S543	975	328	1035	S493	225	328
936	S592	1710	453	986	S542	960	453	1036	S492	210	453
937	S591	1695	328	987	S541	945	328	1037	S491	195	328
938	S590	1680	453	988	S540	930	453	1038	S490	180	453
939	S589	1665	328	989	S539	915	328	1039	S489	165	328
940	S588	1650	453	990	S538	900	453	1040	S488	150	453
941	S587	1635	328	991	S537	885	328	1041	S487	135	328
942	S586	1620	453	992	S536	870	453	1042	S486	120	453
943	S585	1605	328	993	S535	855	328	1043	S485	105	328
944	S584	1590	453	994	S534	840	453	1044	S484	90	453
945	S583	1575	328	995	S533	825	328	1045	S483	75	328
946	S582	1560	453	996	S532	810	453	1046	S482	60	453
947	S581	1545	328	997	S531	795	328	1047	S481	45	328
948	S580	1530	453	998	S530	780	453	1048	DUMMY20	30	453
949	S579	1515	328	999	S529	765	328	1049	DUMMY21	15	328
950	S578	1500	453	1000	S528	750	453	1050	DUMMY22	0	453

No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)
1051	DUMMY23	-15	328	1101	S432	-765	328	1151	S382	-1515	328
1052	DUMMY24	-30	453	1102	S431	-780	453	1152	S381	-1530	453
1053	S480	-45	328	1103	S430	-795	328	1153	S380	-1545	328
1054	S479	-60	453	1104	S429	-810	453	1154	S379	-1560	453
1055	S478	-75	328	1105	S428	-825	328	1155	S378	-1575	328
1056	S477	-90	453	1106	S427	-840	453	1156	S377	-1590	453
1057	S476	-105	328	1107	S426	-855	328	1157	S376	-1605	328
1058	S475	-120	453	1108	S425	-870	453	1158	S375	-1620	453
1059	S474	-135	328	1109	S424	-885	328	1159	S374	-1635	328
1060	S473	-150	453	1110	S423	-900	453	1160	S373	-1650	453
1061	S472	-165	328	1111	S422	-915	328	1161	S372	-1665	328
1062	S471	-180	453	1112	S421	-930	453	1162	S371	-1680	453
1063	S470	-195	328	1113	S420	-945	328	1163	S370	-1695	328
1064	S469	-210	453	1114	S419	-960	453	1164	S369	-1710	453
1065	S468	-225	328	1115	S418	-975	328	1165	S368	-1725	328
1066	S467	-240	453	1116	S417	-990	453	1166	S367	-1740	453
1067	S466	-255	328	1117	S416	-1005	328	1167	S366	-1755	328
1068	S465	-270	453	1118	S415	-1020	453	1168	S365	-1770	453
1069	S464	-285	328	1119	S414	-1035	328	1169	S364	-1785	328
1070	S463	-300	453	1120	S413	-1050	453	1170	S363	-1800	453
1071	S462	-315	328	1121	S412	-1065	328	1171	S362	-1815	328
1072	S461	-330	453	1122	S411	-1080	453	1172	S361	-1830	453
1073	S460	-345	328	1123	S410	-1095	328	1173	S360	-1845	328
1074	S459	-360	453	1124	S409	-1110	453	1174	S359	-1860	453
1075	S458	-375	328	1125	S408	-1125	328	1175	S358	-1875	328
1076	S457	-390	453	1126	S407	-1140	453	1176	S357	-1890	453
1077	S456	-405	328	1127	S406	-1155	328	1177	S356	-1905	328
1078	S455	-420	453	1128	S405	-1170	453	1178	S355	-1920	453
1079	S454	-435	328	1129	S404	-1185	328	1179	S354	-1935	328
1080	S453	-450	453	1130	S403	-1200	453	1180	S353	-1950	453
1081	S452	-465	328	1131	S402	-1215	328	1181	S352	-1965	328
1082	S451	-480	453	1132	S401	-1230	453	1182	S351	-1980	453
1083	S450	-495	328	1133	S400	-1245	328	1183	S350	-1995	328
1084	S449	-510	453	1134	S399	-1260	453	1184	S349	-2010	453
1085	S448	-525	328	1135	S398	-1275	328	1185	S348	-2025	328
1086	S447	-540	453	1136	S397	-1290	453	1186	S347	-2040	453
1087	S446	-555	328	1137	S396	-1305	328	1187	S346	-2055	328
1088	S445	-570	453	1138	S395	-1320	453	1188	S345	-2070	453
1089	S444	-585	328	1139	S394	-1335	328	1189	S344	-2085	328
1090	S443	-600	453	1140	S393	-1350	453	1190	S343	-2100	453
1091	S442	-615	328	1141	S392	-1365	328	1191	S342	-2115	328
1092	S441	-630	453	1142	S391	-1380	453	1192	S341	-2130	453
1093	S440	-645	328	1143	S390	-1395	328	1193	S340	-2145	328
1094	S439	-660	453	1144	S389	-1410	453	1194	S339	-2160	453
1095	S438	-675	328	1145	S388	-1425	328	1195	S338	-2175	328
1096	S437	-690	453	1146	S387	-1440	453	1196	S337	-2190	453
1097	S436	-705	328	1147	S386	-1455	328	1197	S336	-2205	328
1098	S435	-720	453	1148	S385	-1470	453	1198	S335	-2220	453
1099	S434	-735	328	1149	S384	-1485	328	1199	S334	-2235	328
1100	S433	-750	453	1150	S383	-1500	453	1200	S333	-2250	453

No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)
1201	S332	-2265	328	1251	S282	-3015	328	1301	S232	-3765	328
1202	S331	-2280	453	1252	S281	-3030	453	1302	S231	-3780	453
1203	S330	-2295	328	1253	S280	-3045	328	1303	S230	-3795	328
1204	S329	-2310	453	1254	S279	-3060	453	1304	S229	-3810	453
1205	S328	-2325	328	1255	S278	-3075	328	1305	S228	-3825	328
1206	S327	-2340	453	1256	S277	-3090	453	1306	S227	-3840	453
1207	S326	-2355	328	1257	S276	-3105	328	1307	S226	-3855	328
1208	S325	-2370	453	1258	S275	-3120	453	1308	S225	-3870	453
1209	S324	-2385	328	1259	S274	-3135	328	1309	S224	-3885	328
1210	S323	-2400	453	1260	S273	-3150	453	1310	S223	-3900	453
1211	S322	-2415	328	1261	S272	-3165	328	1311	S222	-3915	328
1212	S321	-2430	453	1262	S271	-3180	453	1312	S221	-3930	453
1213	S320	-2445	328	1263	S270	-3195	328	1313	S220	-3945	328
1214	S319	-2460	453	1264	S269	-3210	453	1314	S219	-3960	453
1215	S318	-2475	328	1265	S268	-3225	328	1315	S218	-3975	328
1216	S317	-2490	453	1266	S267	-3240	453	1316	S217	-3990	453
1217	S316	-2505	328	1267	S266	-3255	328	1317	S216	-4005	328
1218	S315	-2520	453	1268	S265	-3270	453	1318	S215	-4020	453
1219	S314	-2535	328	1269	S264	-3285	328	1319	S214	-4035	328
1220	S313	-2550	453	1270	S263	-3300	453	1320	S213	-4050	453
1221	S312	-2565	328	1271	S262	-3315	328	1321	S212	-4065	328
1222	S311	-2580	453	1272	S261	-3330	453	1322	S211	-4080	453
1223	S310	-2595	328	1273	S260	-3345	328	1323	S210	-4095	328
1224	S309	-2610	453	1274	S259	-3360	453	1324	S209	-4110	453
1225	S308	-2625	328	1275	S258	-3375	328	1325	S208	-4125	328
1226	S307	-2640	453	1276	S257	-3390	453	1326	S207	-4140	453
1227	S306	-2655	328	1277	S256	-3405	328	1327	S206	-4155	328
1228	S305	-2670	453	1278	S255	-3420	453	1328	S205	-4170	453
1229	S304	-2685	328	1279	S254	-3435	328	1329	S204	-4185	328
1230	S303	-2700	453	1280	S253	-3450	453	1330	S203	-4200	453
1231	S302	-2715	328	1281	S252	-3465	328	1331	S202	-4215	328
1232	S301	-2730	453	1282	S251	-3480	453	1332	S201	-4230	453
1233	S300	-2745	328	1283	S250	-3495	328	1333	S200	-4245	328
1234	S299	-2760	453	1284	S249	-3510	453	1334	S199	-4260	453
1235	S298	-2775	328	1285	S248	-3525	328	1335	S198	-4275	328
1236	S297	-2790	453	1286	S247	-3540	453	1336	S197	-4290	453
1237	S296	-2805	328	1287	S246	-3555	328	1337	S196	-4305	328
1238	S295	-2820	453	1288	S245	-3570	453	1338	S195	-4320	453
1239	S294	-2835	328	1289	S244	-3585	328	1339	S194	-4335	328
1240	S293	-2850	453	1290	S243	-3600	453	1340	S193	-4350	453
1241	S292	-2865	328	1291	S242	-3615	328	1341	S192	-4365	328
1242	S291	-2880	453	1292	S241	-3630	453	1342	S191	-4380	453
1243	S290	-2895	328	1293	S240	-3645	328	1343	S190	-4395	328
1244	S289	-2910	453	1294	S239	-3660	453	1344	S189	-4410	453
1245	S288	-2925	328	1295	S238	-3675	328	1345	S188	-4425	328
1246	S287	-2940	453	1296	S237	-3690	453	1346	S187	-4440	453
1247	S286	-2955	328	1297	S236	-3705	328	1347	S186	-4455	328
1248	S285	-2970	453	1298	S235	-3720	453	1348	S185	-4470	453
1249	S284	-2985	328	1299	S234	-3735	328	1349	S184	-4485	328
1250	S283	-3000	453	1300	S233	-3750	453	1350	S183	-4500	453

No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)
1351	S182	-4515	328	1401	S132	-5265	328	1451	S82	-6015	328
1352	S181	-4530	453	1402	S131	-5280	453	1452	S81	-6030	453
1353	S180	-4545	328	1403	S130	-5295	328	1453	S80	-6045	328
1354	S179	-4560	453	1404	S129	-5310	453	1454	S79	-6060	453
1355	S178	-4575	328	1405	S128	-5325	328	1455	S78	-6075	328
1356	S177	-4590	453	1406	S127	-5340	453	1456	S77	-6090	453
1357	S176	-4605	328	1407	S126	-5355	328	1457	S76	-6105	328
1358	S175	-4620	453	1408	S125	-5370	453	1458	S75	-6120	453
1359	S174	-4635	328	1409	S124	-5385	328	1459	S74	-6135	328
1360	S173	-4650	453	1410	S123	-5400	453	1460	S73	-6150	453
1361	S172	-4665	328	1411	S122	-5415	328	1461	S72	-6165	328
1362	S171	-4680	453	1412	S121	-5430	453	1462	S71	-6180	453
1363	S170	-4695	328	1413	S120	-5445	328	1463	S70	-6195	328
1364	S169	-4710	453	1414	S119	-5460	453	1464	S69	-6210	453
1365	S168	-4725	328	1415	S118	-5475	328	1465	S68	-6225	328
1366	S167	-4740	453	1416	S117	-5490	453	1466	S67	-6240	453
1367	S166	-4755	328	1417	S116	-5505	328	1467	S66	-6255	328
1368	S165	-4770	453	1418	S115	-5520	453	1468	S65	-6270	453
1369	S164	-4785	328	1419	S114	-5535	328	1469	S64	-6285	328
1370	S163	-4800	453	1420	S113	-5550	453	1470	S63	-6300	453
1371	S162	-4815	328	1421	S112	-5565	328	1471	S62	-6315	328
1372	S161	-4830	453	1422	S111	-5580	453	1472	S61	-6330	453
1373	S160	-4845	328	1423	S110	-5595	328	1473	S60	-6345	328
1374	S159	-4860	453	1424	S109	-5610	453	1474	S59	-6360	453
1375	S158	-4875	328	1425	S108	-5625	328	1475	S58	-6375	328
1376	S157	-4890	453	1426	S107	-5640	453	1476	S57	-6390	453
1377	S156	-4905	328	1427	S106	-5655	328	1477	S56	-6405	328
1378	S155	-4920	453	1428	S105	-5670	453	1478	S55	-6420	453
1379	S154	-4935	328	1429	S104	-5685	328	1479	S54	-6435	328
1380	S153	-4950	453	1430	S103	-5700	453	1480	S53	-6450	453
1381	S152	-4965	328	1431	S102	-5715	328	1481	S52	-6465	328
1382	S151	-4980	453	1432	S101	-5730	453	1482	S51	-6480	453
1383	S150	-4995	328	1433	S100	-5745	328	1483	S50	-6495	328
1384	S149	-5010	453	1434	S99	-5760	453	1484	S49	-6510	453
1385	S148	-5025	328	1435	S98	-5775	328	1485	S48	-6525	328
1386	S147	-5040	453	1436	S97	-5790	453	1486	S47	-6540	453
1387	S146	-5055	328	1437	S96	-5805	328	1487	S46	-6555	328
1388	S145	-5070	453	1438	S95	-5820	453	1488	S45	-6570	453
1389	S144	-5085	328	1439	S94	-5835	328	1489	S44	-6585	328
1390	S143	-5100	453	1440	S93	-5850	453	1490	S43	-6600	453
1391	S142	-5115	328	1441	S92	-5865	328	1491	S42	-6615	328
1392	S141	-5130	453	1442	S91	-5880	453	1492	S41	-6630	453
1393	S140	-5145	328	1443	S90	-5895	328	1493	S40	-6645	328
1394	S139	-5160	453	1444	S89	-5910	453	1494	S39	-6660	453
1395	S138	-5175	328	1445	S88	-5925	328	1495	S38	-6675	328
1396	S137	-5190	453	1446	S87	-5940	453	1496	S37	-6690	453
1397	S136	-5205	328	1447	S86	-5955	328	1497	S36	-6705	328
1398	S135	-5220	453	1448	S85	-5970	453	1498	S35	-6720	453
1399	S134	-5235	328	1449	S84	-5985	328	1499	S34	-6735	328
1400	S133	-5250	453	1450	S83	-6000	453	1500	S33	-6750	453

No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)
1501	S32	-6765	328	1551	G458	-7515	328	1601	G358	-8265	328
1502	S31	-6780	453	1552	G456	-7530	453	1602	G356	-8280	453
1503	S30	-6795	328	1553	G454	-7545	328	1603	G354	-8295	328
1504	S29	-6810	453	1554	G452	-7560	453	1604	G352	-8310	453
1505	S28	-6825	328	1555	G450	-7575	328	1605	G350	-8325	328
1506	S27	-6840	453	1556	G448	-7590	453	1606	G348	-8340	453
1507	S26	-6855	328	1557	G446	-7605	328	1607	G346	-8355	328
1508	S25	-6870	453	1558	G444	-7620	453	1608	G344	-8370	453
1509	S24	-6885	328	1559	G442	-7635	328	1609	G342	-8385	328
1510	S23	-6900	453	1560	G440	-7650	453	1610	G340	-8400	453
1511	S22	-6915	328	1561	G438	-7665	328	1611	G338	-8415	328
1512	S21	-6930	453	1562	G436	-7680	453	1612	G336	-8430	453
1513	S20	-6945	328	1563	G434	-7695	328	1613	G334	-8445	328
1514	S19	-6960	453	1564	G432	-7710	453	1614	G332	-8460	453
1515	S18	-6975	328	1565	G430	-7725	328	1615	G330	-8475	328
1516	S17	-6990	453	1566	G428	-7740	453	1616	G328	-8490	453
1517	S16	-7005	328	1567	G426	-7755	328	1617	G326	-8505	328
1518	S15	-7020	453	1568	G424	-7770	453	1618	G324	-8520	453
1519	S14	-7035	328	1569	G422	-7785	328	1619	G322	-8535	328
1520	S13	-7050	453	1570	G420	-7800	453	1620	G320	-8550	453
1521	S12	-7065	328	1571	G418	-7815	328	1621	G318	-8565	328
1522	S11	-7080	453	1572	G416	-7830	453	1622	G316	-8580	453
1523	S10	-7095	328	1573	G414	-7845	328	1623	G314	-8595	328
1524	S9	-7110	453	1574	G412	-7860	453	1624	G312	-8610	453
1525	S8	-7125	328	1575	G410	-7875	328	1625	G310	-8625	328
1526	S7	-7140	453	1576	G408	-7890	453	1626	G308	-8640	453
1527	S6	-7155	328	1577	G406	-7905	328	1627	G306	-8655	328
1528	S5	-7170	453	1578	G404	-7920	453	1628	G304	-8670	453
1529	S4	-7185	328	1579	G402	-7935	328	1629	G302	-8685	328
1530	S3	-7200	453	1580	G400	-7950	453	1630	G300	-8700	453
1531	S2	-7215	328	1581	G398	-7965	328	1631	G298	-8715	328
1532	S1	-7230	453	1582	G396	-7980	453	1632	G296	-8730	453
1533	DUMMY25	-7245	328	1583	G394	-7995	328	1633	G294	-8745	328
1534	DUMMY26	-7260	453	1584	G392	-8010	453	1634	G292	-8760	453
1535	DUMMY27	-7275	328	1585	G390	-8025	328	1635	G290	-8775	328
1536	DUMMY28	-7290	453	1586	G388	-8040	453	1636	G288	-8790	453
1537	DUMMY29	-7305	328	1587	G386	-8055	328	1637	G286	-8805	328
1538	DUMMY30	-7320	453	1588	G384	-8070	453	1638	G284	-8820	453
1539	DUMMY31	-7335	328	1589	G382	-8085	328	1639	G282	-8835	328
1540	G480	-7350	453	1590	G380	-8100	453	1640	G280	-8850	453
1541	G478	-7365	328	1591	G378	-8115	328	1641	G278	-8865	328
1542	G476	-7380	453	1592	G376	-8130	453	1642	G276	-8880	453
1543	G474	-7395	328	1593	G374	-8145	328	1643	G274	-8895	328
1544	G472	-7410	453	1594	G372	-8160	453	1644	G272	-8910	453
1545	G470	-7425	328	1595	G370	-8175	328	1645	G270	-8925	328
1546	G468	-7440	453	1596	G368	-8190	453	1646	G268	-8940	453
1547	G466	-7455	328	1597	G366	-8205	328	1647	G266	-8955	328
1548	G464	-7470	453	1598	G364	-8220	453	1648	G264	-8970	453
1549	G462	-7485	328	1599	G362	-8235	328	1649	G262	-8985	328
1550	G460	-7500	453	1600	G360	-8250	453	1650	G260	-9000	453

No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)	No.	PIN NAME	X(um)	Y(um)
1651	G258	-9015	328	1701	G158	-9765	328	1751	G58	-10515	328
1652	G256	-9030	453	1702	G156	-9780	453	1752	G56	-10530	453
1653	G254	-9045	328	1703	G154	-9795	328	1753	G54	-10545	328
1654	G252	-9060	453	1704	G152	-9810	453	1754	G52	-10560	453
1655	G250	-9075	328	1705	G150	-9825	328	1755	G50	-10575	328
1656	G248	-9090	453	1706	G148	-9840	453	1756	G48	-10590	453
1657	G246	-9105	328	1707	G146	-9855	328	1757	G46	-10605	328
1658	G244	-9120	453	1708	G144	-9870	453	1758	G44	-10620	453
1659	G242	-9135	328	1709	G142	-9885	328	1759	G42	-10635	328
1660	G240	-9150	453	1710	G140	-9900	453	1760	G40	-10650	453
1661	G238	-9165	328	1711	G138	-9915	328	1761	G38	-10665	328
1662	G236	-9180	453	1712	G136	-9930	453	1762	G36	-10680	453
1663	G234	-9195	328	1713	G134	-9945	328	1763	G34	-10695	328
1664	G232	-9210	453	1714	G132	-9960	453	1764	G32	-10710	453
1665	G230	-9225	328	1715	G130	-9975	328	1765	G30	-10725	328
1666	G228	-9240	453	1716	G128	-9990	453	1766	G28	-10740	453
1667	G226	-9255	328	1717	G126	-10005	328	1767	G26	-10755	328
1668	G224	-9270	453	1718	G124	-10020	453	1768	G24	-10770	453
1669	G222	-9285	328	1719	G122	-10035	328	1769	G22	-10785	328
1670	G220	-9300	453	1720	G120	-10050	453	1770	G20	-10800	453
1671	G218	-9315	328	1721	G118	-10065	328	1771	G18	-10815	328
1672	G216	-9330	453	1722	G116	-10080	453	1772	G16	-10830	453
1673	G214	-9345	328	1723	G114	-10095	328	1773	G14	-10845	328
1674	G212	-9360	453	1724	G112	-10110	453	1774	G12	-10860	453
1675	G210	-9375	328	1725	G110	-10125	328	1775	G10	-10875	328
1676	G208	-9390	453	1726	G108	-10140	453	1776	G8	-10890	453
1677	G206	-9405	328	1727	G106	-10155	328	1777	G6	-10905	328
1678	G204	-9420	453	1728	G104	-10170	453	1778	G4	-10920	453
1679	G202	-9435	328	1729	G102	-10185	328	1779	DUMMY32	-10935	328
1680	G200	-9450	453	1730	G100	-10200	453	1780	G2	-10950	453
1681	G198	-9465	328	1731	G98	-10215	328	1781	DUMMY33	-10965	328
1682	G196	-9480	453	1732	G96	-10230	453	1782	DUMMY34	-10980	453
1683	G194	-9495	328	1733	G94	-10245	328	1783	KEY_1 LEFT	-11110	430
1684	G192	-9510	453	1734	G92	-10260	453				
1685	G190	-9525	328	1735	G90	-10275	328				
1686	G188	-9540	453	1736	G88	-10290	453				
1687	G186	-9555	328	1737	G86	-10305	328				
1688	G184	-9570	453	1738	G84	-10320	453				
1689	G182	-9585	328	1739	G82	-10335	328				
1690	G180	-9600	453	1740	G80	-10350	453				
1691	G178	-9615	328	1741	G78	-10365	328				
1692	G176	-9630	453	1742	G76	-10380	453				
1693	G174	-9645	328	1743	G74	-10395	328				
1694	G172	-9660	453	1744	G72	-10410	453				
1695	G170	-9675	328	1745	G70	-10425	328				
1696	G168	-9690	453	1746	G68	-10440	453				
1697	G166	-9705	328	1747	G66	-10455	328				
1698	G164	-9720	453	1748	G64	-10470	453				
1699	G162	-9735	328	1749	G62	-10485	328				
1700	G160	-9750	453	1750	G60	-10500	453				

5. Pin Description

5.1. Pin Assignment

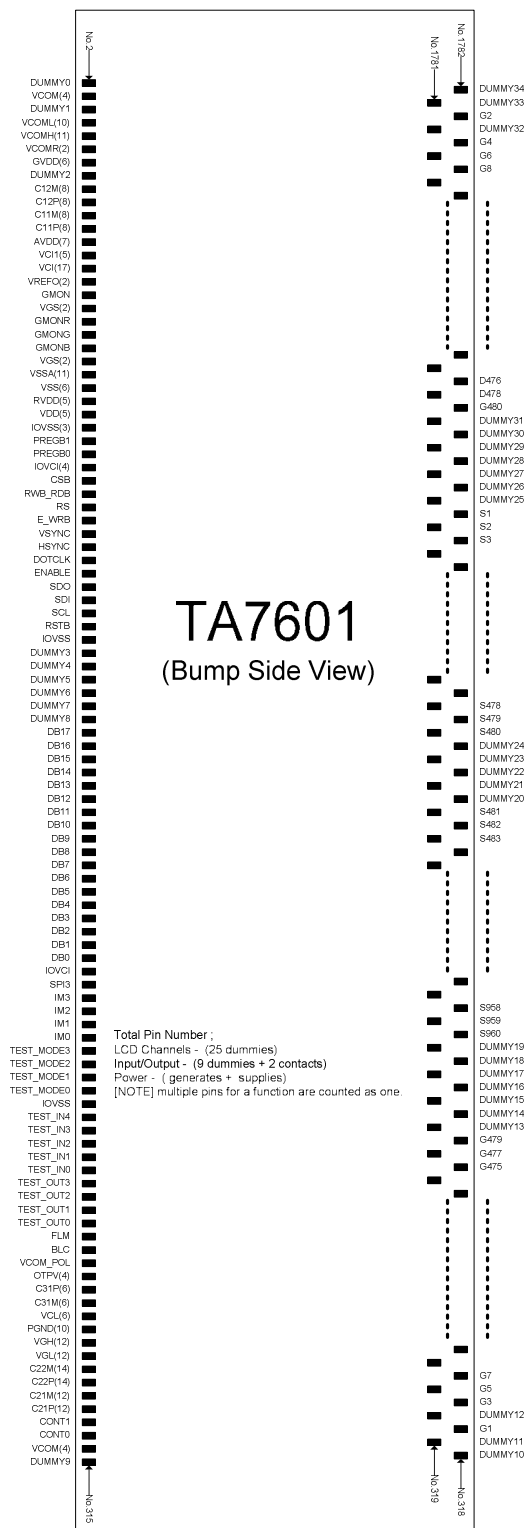


Figure 5-1 : Pin Assignment of TA7601

5.2. Power Supply Pins

Signals	I/O	Voltage level	Description
VDD	I power	1.5V typical	Logic power supply (1.35V to 1.65V). Connect to RVDD on FPC. Don't apply any external power to this pin.
RVDD	O power	1.5V typical	1.5V Regulator output. VDD and RVDD must have equal potential. Connect to VDD on FPC.
			Connect a capacitor for stabilization on FPC.
VCI	I power	2.5 to 3.3V	Analog power supply (2.5V to 3.3V, Typ.2.8V)
IOVCI	I power	1.65 to 3.3V	I/O power supply for external interface (1.65V to 3.3V).
VSS	I power	0V	Ground for logic.
VSSA	I power	0V	Ground for source driver block.
IOVSS	I power	0V	Ground for I/O
AVDD	O power	4.5 to 5.5V	Power output that is generated in power block for source and VCOM block (4.5V to 5.5V).
GVDD	O power	3.0 to 5.0V	Reference voltage level for grayscale voltage generator. Connect a capacitor for stabilization
PGND	I power	0V	Equal level to VSSA (short to VSSA internally)

Signals	I/O	Voltage level	Description
VCI1	O power	1.7 to 3.0V	Reference voltage for step-up circuit 1(DCDC1). The VCI1 output level is set with the VC[3:0] bits. Connect a capacitor for stabilization on FPC.
VREFO	O	2.0V	Reference voltage for generating GVDD, VCOMH, VCOML, VCI1
VCOMH	O	3.0 to 5.0V	The high level of VCOM AC voltage. Adjust VCOMH with either internal electric volumes or an external resistor from VCOMR. Connect a capacitor for stabilization on FPC.
VCOML	O	(VCL+0.5) to 1V	The low level of VCOM AC voltage. Adjust VCOML with the VML bits. To fix the VCOML level to GND, set VCOMG=0. In this case, capacitor connection is not necessary. $VCOML=(VCL+0.5)V$ to 1V.
VCOMR	I/O	1.2V to 2.0V	VCOMR is used when adjusting the VCOMH level with an external resistor. Place a variable resistor between GVDD and GND, or between VREFO and GND.
VGS	I power	GND or Resistor	A reference level for the grayscale voltage generating circuit. Connected to GND or Resister
VGH	O power	Max. = 19.25V	A supply voltage to gate drivers incorporated in a TFT LCD panel. This voltage is generated from VCI1 and AVDD from the step-up circuit 2 (DCDC2). The step-up rate is set with the BT bits. $VGH = \max. 19.25V$ Connect capacitor for stabilization on FPC. ($Vop(VGH - VGL) \leq 27V$)
VGL	O power	Min. = -13.75V	A supply voltage to gate drivers incorporated in a TFT LCD panel. An output voltage generated from VCI1 and AVDD from the step-up circuit 2. The step-up rate is set with the BT bits. $VGL = \min. -13.75V$. Connect capacitor for stabilization on FPC. ($Vop(VGH - VGL) \leq 27V$)
VCL	O power	0V to -2.75V	Power supply for generating VCOML. An output voltage from the step-up circuit 3 (DCDC3)
OTP	I power	TBD	Power supply for OTP programming. When using OTP programming, external power supply should be applied to this pin. After OTP programming, external power supply must be removed and leave this pin open. Leave this open if not in use.

5.3. Logic I/O Pins

Signals	I/O	To / From	Description																				
IM3 IM2 IM1 IM0/ID	I	VSS/ IOVCI	Select the MPU interface mode as listed below.																				
			IM[3:0]	Description																			
			4'b0000	M68, 16-bit bus interface																			
			4'b0001	M68, 8-bit bus interface																			
			4'b0010	I80, 16-bit bus interface																			
			4'b0011	I80, 8-bit bus interface																			
			4'b010x	Serial peripheral interface, 16-bit stream IM[0] → ID																			
			4'b011x	Serial peripheral interface, 18-bit stream IM[0] → ID																			
			4'b1000	M68, 18-bit bus interface																			
			4'b1001	M68, 9-bit bus interface																			
			4'b1010	I80, 18-bit bus interface																			
			4'b1011	I80, 9-bit bus interface																			
			4'b1100	Reserved																			
			4'b1110	Reserved																			
			4'b1101	Reserved																			
			4'b1111	Reserved																			
			Note: When the serial interface is selected, the IM0 pin is used as an ID bit of the device code.																				
CSB	I	MPU	Chip select signal. Low: the chip can be accessed. High: the chip cannot be accessed. Must be connected to IOVCI if not in use.																				
RS	I	MPU	The signal for register index or register command select. Low: Register index or internal status (in read operation) High: Register command. Connect to IOVCI or VSS level when the serial data transfer interface is selected.																				
E_WRB	I	MPU	In M68 mode, this serves as a write/read enable strobe (E). In I80 mode, this serves as a write strobe signal (WRB).																				
RWB_RDB	I	MPU	In M68 mode, this is used to select operation, read or write (RWB). In I80 mode, this serves as a read strobe signal (RDB). Fix this pin to the IOVCI or VSS level when using the serial data transfer interface.																				
ENABLE	I	MPU	A data ENABLE signal in the RGB I/F mode. Fix the unused pin to either the VSS level or the IOVCI level. Low: Selected (access enabled) The polarity of the ENABLE signal is inverted by the EPL bit. <table><tr><th>EPL</th><th>ENABLE</th><th>DDRAM write</th><th>DDRAM address</th></tr><tr><td>0</td><td>0</td><td>Enable</td><td>Update</td></tr><tr><td>0</td><td>1</td><td>Disable</td><td>Retained</td></tr><tr><td>1</td><td>0</td><td>Disable</td><td>Retained</td></tr><tr><td>1</td><td>1</td><td>Enable</td><td>Update</td></tr></table>	EPL	ENABLE	DDRAM write	DDRAM address	0	0	Enable	Update	0	1	Disable	Retained	1	0	Disable	Retained	1	1	Enable	Update
EPL	ENABLE	DDRAM write	DDRAM address																				
0	0	Enable	Update																				
0	1	Disable	Retained																				
1	0	Disable	Retained																				
1	1	Enable	Update																				
VSYNC	I	MPU	Frame synchronizing signal. Fix this pin to the IOVCI level when not in use. If VSPL=0: Active low. If VSPL=1: Active high.																				
HSYNC	I	MPU	Horizontal Line synchronizing signal. Fix this pin to the IOVCI level when not in use. If HSPL=0: Active low. If HSPL=1: Active high.																				

Signals	I/O	To / From	Description																																																																								
DOTCLK	I	MPU	Dot clock signal. Fix this pin to the IOVCI level when not in use. If DPL=0: Data are input on the rising edge of DOTCLK. If DPL=1: Data are input on the falling edge of DOTCLK.																																																																								
RSTB	I	MPU or reset circuit	Reset pin. Setting this pin to low initializes the LSI. Must be reset after power is supplied.																																																																								
SDI	I/O	MPU	Serial data transfer input/output in the serial data transfer interface mode. Data is input on the rising edge of the SCL signal. If SPI3 = 0, only input pin If SPI3 = 1, bidirectional pin Fix this pin to IOVCI when not in use. In this case, SPI3 should be "0".																																																																								
SDO	O	MPU	Serial data transfer output in the serial data transfer interface mode. Data is output on the falling edge of the SCL signal Leave this pin open if not in use.																																																																								
SCL	I	MPU	In SPI mode, this serves as a synchronous clock (SCL).																																																																								
SPI3	I	VSS/ IOVCI	Mode selection pin for Serial Peripheral Interface. If SPI3 = 0, 4-wire SPI mode If SPI3 = 1, 3-wire SPI mode. That is, SDI is bidirectional pin.																																																																								
DB[17:0]	I/O	MPU	<div>Data bus for SYSTEM I/F<table><tr><th colspan="2">Interface Mode</th><th colspan="2">Description</th></tr><tr><th>IM[3:0]</th><th>Description</th><th>Index</th><th>Data</th></tr><tr><td>4'b0000</td><td>M68, 16-bit bus interface</td><td>DB[8:1]</td><td>DB[17:10],DB[8:1]</td></tr><tr><td>4'b0001</td><td>M68, 8-bit bus interface</td><td>DB[17:10]</td><td>DB[17:10]</td></tr><tr><td>4'b0010</td><td>I80, 16-bit bus interface</td><td>DB[8:1]</td><td>DB[17:10],DB[8:1]</td></tr><tr><td>4'b0011</td><td>I80, 8-bit bus interface</td><td>DB[17:10]</td><td>DB[17:10]</td></tr><tr><td>4'b010x</td><td>Serial peripheral interface</td><td>-</td><td>-</td></tr><tr><td>4'b011x</td><td>Serial peripheral interface</td><td>-</td><td>-</td></tr><tr><td>4'b1000</td><td>M68, 18-bit bus interface</td><td>DB[8:1]</td><td>DB[17:0]</td></tr><tr><td>4'b1001</td><td>M68, 9-bit bus interface</td><td>DB[17:10]</td><td>DB[17:9]</td></tr><tr><td>4'b1010</td><td>I80, 18-bit bus interface</td><td>DB[8:1]</td><td>DB[17:0]</td></tr><tr><td>4'b1011</td><td>I80, 9-bit bus interface</td><td>DB[17:10]</td><td>DB[17:9]</td></tr><tr><td>4'b1100</td><td>Reserved</td><td>-</td><td>-</td></tr><tr><td>4'b1110</td><td>Reserved</td><td>-</td><td>-</td></tr><tr><td>4'b1101</td><td>Reserved</td><td>-</td><td>-</td></tr><tr><td>4'b1111</td><td>Reserved</td><td>-</td><td>-</td></tr></table></div> <div>Data bus for RGB I/F<table><tr><th>Interface Mode</th><th>Description</th></tr><tr><td>6-bit interface, 3-transfer</td><td>DB[17:12]</td></tr><tr><td>16-bit interface, 1-transfer</td><td>DB[17:13],DB[11:1]</td></tr><tr><td>18-bit interface, 1-transfer</td><td>DB[17:0]</td></tr></table></div> <div>Connected unused pins to the IOVCI or VSS level</div>	Interface Mode		Description		IM[3:0]	Description	Index	Data	4'b0000	M68, 16-bit bus interface	DB[8:1]	DB[17:10],DB[8:1]	4'b0001	M68, 8-bit bus interface	DB[17:10]	DB[17:10]	4'b0010	I80, 16-bit bus interface	DB[8:1]	DB[17:10],DB[8:1]	4'b0011	I80, 8-bit bus interface	DB[17:10]	DB[17:10]	4'b010x	Serial peripheral interface	-	-	4'b011x	Serial peripheral interface	-	-	4'b1000	M68, 18-bit bus interface	DB[8:1]	DB[17:0]	4'b1001	M68, 9-bit bus interface	DB[17:10]	DB[17:9]	4'b1010	I80, 18-bit bus interface	DB[8:1]	DB[17:0]	4'b1011	I80, 9-bit bus interface	DB[17:10]	DB[17:9]	4'b1100	Reserved	-	-	4'b1110	Reserved	-	-	4'b1101	Reserved	-	-	4'b1111	Reserved	-	-	Interface Mode	Description	6-bit interface, 3-transfer	DB[17:12]	16-bit interface, 1-transfer	DB[17:13],DB[11:1]	18-bit interface, 1-transfer	DB[17:0]
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4'b1011	I80, 9-bit bus interface	DB[17:10]	DB[17:9]																																																																								
4'b1100	Reserved	-	-																																																																								
4'b1110	Reserved	-	-																																																																								
4'b1101	Reserved	-	-																																																																								
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16-bit interface, 1-transfer	DB[17:13],DB[11:1]																																																																										
18-bit interface, 1-transfer	DB[17:0]																																																																										

Signals	I/O	To / From	Description
FLM	O	MPU	Output a frame head pulse signal. (amplitude : IOVCI-GND). The FLM signal is used when writing DDRAM data in synchronization with a frame. Leave this pin open if not in use.
BLC	O	White LED driver	PWM signal for back light control. (amplitude : IOVCI-GND) Freq. range of PWM signal : 520Hz ~ 20KHz (TBD) Leave this pin open if not in use.
VCOM_POL	O	MPU	Output polarity of VCOM. (amplitude : IOVCI-GND). Leave this pin open if not in use.

5.4. Step-up Capacitor Pins

Signals	Description
C11P	Capacitor connection pin for step-up circuit1(DCDC1)
C11M	Capacitor connection pin for step-up circuit1(DCDC1)
C12P	Capacitor connection pin for step-up circuit1(DCDC1)
C12M	Capacitor connection pin for step-up circuit1(DCDC1)
C21P	Capacitor connection pin for step-up circuit2(DCDC 2)
C21M	Capacitor connection pin for step-up circuit2(DCDC 2)
C22P	Capacitor connection pin for step-up circuit2(DCDC 2)
C22M	Capacitor connection pin for step-up circuit2(DCDC 2)
C31P	Capacitor connection pin for step-up circuit3(DCDC 3)
C31M	Capacitor connection pin for step-up circuit3(DCDC 3)

5.5. Display Output Pins

Signals	Name	I/O	Connected to	Function	Status not to be used
S[960:1]	Source output	O	LCD	Output voltages applied to the liquid crystal. The shift direction of segment signal outputs is changeable with the SS bit. For example, when SS=0, S1 outputs the DDRAM address "0000" data. When SS=1, S960 outputs the DDRAM address "0000" data. S1, S4, S7...display red I, (SS=0) S2, S5, S8...display green (G), (SS=0) S3, S6, S9...display blue (B), (SS=0)	Open
G[480:1]	Gate output	O	LCD	Gate line output pins The output of circuit is either VGH or VGL VGH : gate-ON level VGL : gate-OFF level	Open
VCOM	VCOM output	O	LCD	Pins for the VCOM output These are short-circuited within the chip.	Open

5.6. Test Pins and Others

Signals	I/O	Function	Status not to be used
TEST_MODE [3:0]	I	Test pin. In normal operation, fix to GND level.	GND
TEST_IN[4:0]	I	Test input. In normal operation, fix to GND level.	GND
TEST_OUT[3:0]	O	Test output.	Open
PREGB[1:0]	I	PREGB[1] should be tied to "low" and PREGB[0] should be tied to "high".	GND
CONTACT1 CONTACT2	O	Dummy pins. Use them to measure the COG contact resistance CONTACT1 and CONTACT2 are short-circuited within the chip	Open
DUMMY1, DUMMY2	O	Dummy pins. Leave these pins open	Open
DUMMY3~DUMMY8	I	Should be tied to "low"	GND
DUMMY9~DUMMY34	O	Dummy pins. Leave these pins open	Open
GMON	O	Test output (to monitor gamma voltage)	Open

6. Functional Description

6.1. System interface

D51E5TA7601 has 10 high-speed system interfaces : 80-system 18-/16-/9-/8-bit MPU interfaces, 68-system 18-/16-/9-/8-bit MPU interfaces and 16-/18-bit SPI's (Serial Peripheral Interfaces). The IM[3:0] pin determines the interface mode.

Users may write/read data to/from internal DDRAM (Display Data RAM) as well as a lot of internal control registers through these system interfaces.

When users want to access the LSI, they must generate control signals as shown below.

Table 6-1 : Parallel Interface

E WRB	RWB/RDB	RS	Operation
1 / 0	0 / 1	0	Write indexes Index means register address
1 / 1	1 / 0	0	Read internal status
1 / 0	0 / 1	1	Write register data into registers or image data into DDRAM
1 / 1	1 / 0	1	Read data from registers or DDRAM

Table 6-2 : Serial Interface

RWB	RS	Operation
0	0	Write indexes
1	0	Read internal status
0	1	Write register data into registers or image data into DDRAM
1	1	Read data from registers or DDRAM

6.2. RGB interface

The display operation via the RGB interface is synchronized with VSYNC (frame synchronizing signal), HSYNC (line synchronizing signal) and DOTCLK (dot clock). Display data in a pixel unit via the DB[17:0] are written according to the data enable signal (ENABLE) and DOTCLK. The RGB interface can be used by setting RM=1. The interface is selected by setting the RIM[2:0] bit. The RGB interface enables transferring minimum necessary data and rewriting the DDRAM area need to be overwritten with the use of window address function.

6.3. Instruction table

The D51E5TA7601 has an instruction table to control internal operations and many internal analog blocks including Power blocks, Source driver and Gate driver.

6.4. DDRAM (Display Data RAM)

The D51E5TA7601 has the internal DDRAM that stores 345,600-byte bit-pattern data, where one pixel is expressed with 18 bits. The DDRAM address map is as follows:

Table 6-3 : DDRAM Address and Display Panel Position (SS="0", BGR="0")

S/G pin	S1	S2	S3	S4	S5	S6	S7	S8	S9	--	S949	S950	S951	S952	S953	S954	S955	S956	S957	S958	S959	S960
	DB17 – DB0			DB17 – DB0			DB17 – DB0				DB17 – DB0			DB17 – DB0			DB17 – DB0			DB17 – DB0		
G1	(000h, 000h)			(001h, 000h)			(002h, 000h)			---	(13Ch, 000h)			(13Dh, 000h)			(13Eh, 000h)			(13Fh, 000h)		
G2	(000h, 001h)			(001h, 001h)			(002h, 001h)			---	(13Ch, 001h)			(13Dh, 001h)			(13Eh, 001h)			(13Fh, 001h)		
G3	(000h, 002h)			(001h, 002h)			(002h, 002h)			---	(13Ch, 002h)			(13Dh, 002h)			(13Eh, 002h)			(13Fh, 002h)		
G4	(000h, 003h)			(001h, 003h)			(002h, 003h)			---	(13Ch, 003h)			(13Dh, 003h)			(13Eh, 003h)			(13Fh, 003h)		
G5	(000h, 004h)			(001h, 004h)			(002h, 004h)			---	(13Ch, 004h)			(13Dh, 004h)			(13Eh, 004h)			(13Fh, 004h)		
G6	(000h, 005h)			(001h, 005h)			(002h, 005h)			---	(13Ch, 005h)			(13Dh, 005h)			(13Eh, 005h)			(13Fh, 005h)		
G7	(000h, 006h)			(001h, 006h)			(002h, 006h)			---	(13Ch, 006h)			(13Dh, 006h)			(13Eh, 006h)			(13Fh, 006h)		
G8	(000h, 007h)			(001h, 007h)			(002h, 007h)			---	(13Ch, 007h)			(13Dh, 007h)			(13Eh, 007h)			(13Fh, 007h)		
G9	(000h, 008h)			(001h, 008h)			(002h, 008h)			---	(13Ch, 008h)			(13Dh, 008h)			(13Eh, 008h)			(13Fh, 008h)		
G10	(000h, 009h)			(001h, 009h)			(002h, 009h)			---	(13Ch, 009h)			(13Dh, 009h)			(13Eh, 009h)			(13Fh, 009h)		
---	---			---			---			---	---			---			---			---		
G471	(000h, 1D6h)			(001h, 1D6h)			(002h, 1D6h)			---	(13Ch, 1D6h)			(13Dh, 1D6h)			(13Eh, 1D6h)			(13Fh, 1D6h)		
G472	(000h, 1D7h)			(001h, 1D7h)			(002h, 1D7h)			---	(13Ch, 1D7h)			(13Dh, 1D7h)			(13Eh, 1D7h)			(13Fh, 1D7h)		
G473	(000h, 1D8h)			(001h, 1D8h)			(002h, 1D8h)			---	(13Ch, 1D8h)			(13Dh, 1D8h)			(13Eh, 1D8h)			(13Fh, 1D8h)		
G474	(000h, 1D9h)			(001h, 1D9h)			(002h, 1D9h)			---	(13Ch, 1D9h)			(13Dh, 1D9h)			(13Eh, 1D9h)			(13Fh, 1D9h)		
G475	(000h, 1DAh)			(001h, 1DAh)			(002h, 1DAh)			---	(13Ch, 1DAh)			(13Dh, 1DAh)			(13Eh, 1DAh)			(13Fh, 1DAh)		
G476	(000h, 1DBh)			(001h, 1DBh)			(002h, 1DBh)			---	(13Ch, 1DBh)			(13Dh, 1DBh)			(13Eh, 1DBh)			(13Fh, 1DBh)		
G477	(000h, 1DCh)			(001h, 1DCh)			(002h, 1DCh)			---	(13Ch, 1DCh)			(13Dh, 1DCh)			(13Eh, 1DCh)			(13Fh, 1DCh)		
G478	(000h, 1DDh)			(001h, 1DDh)			(002h, 1DDh)			---	(13Ch, 1DDh)			(13Dh, 1DDh)			(13Eh, 1DDh)			(13Fh, 1DDh)		
G479	(000h, 1DEh)			(001h, 1DEh)			(002h, 1DEh)			---	(13Ch, 1DEh)			(13Dh, 1DEh)			(13Eh, 1DEh)			(13Fh, 1DEh)		
G480	(000h, 1DFh)			(001h, 1DFh)			(002h, 1DFh)			---	(13Ch, 1DFh)			(13Dh, 1DFh)			(13Eh, 1DFh)			(13Fh, 1DFh)		

6.5. Grayscale voltage generator

The grayscale voltage circuit generates a certain voltage level that is specified by the grayscale gamma-adjusting resistor for LCD driver circuit. By use of generator, 262,144 colors can be displayed at the same time. For details, see the gamma-adjusting resistor section.

6.6. Timing generator

The timing generator generates timing signals for TFT-LCD driver and control signals for the operation of internal circuits such as source driver and DDRAM. The DDRAM read operations done by this timing generator and DDRAM write operations done through system interface are performed independently to avoid the interference between them.

6.7. Oscillation circuit (OSC)

The device has RC type OSC with built-in capacitor.

During standby mode and deep-standby mode, RC oscillation is halted to reduce power consumption.

6.8. Source driver circuit

The LCD source driver circuit consists of 960 output channels (S1 to S960).

Display data are latched when 960-channel data arrived. The latched data then enables the source driver to generate drive outputs.

6.9. Gate driver circuit

The liquid crystal display gate driver circuit consists of 480 gate drivers (G1 to G480).

The VGH or VGL level is output by the signal from the gate control circuit. The shift direction of gate outputs from the gate driver is controlled by GS register. The scan mode by gate driver is controlled by SM register.

6.10. LCD Drive Power Supply circuit

The LCD drive power supply circuit generates the voltage levels VGH, VGL, VCOMH/VCOML and GVDD for driving a LCD panel.

7. Instructions

Table 7-1 : Instruction Table (to be continued)

	Reg. No	R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	description	default value
Display Control System	SR	R	0	L8	L7	L6	L5	L4	L3	L2	L1	L0	0	0	0	0	0	0	0	status read	x
	R00h	W	1	X	X	X	X	X	X	X	X	X	X	X	S_RST	X	X	X	OSC_ON	start oscillation	16'h0001
		R	1	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	1	device code : 8551	x
	R01h	W	1	VSPL	HSPL	DPL	EPL	X	SM	GS	X	X	X	NL[5]	NL[4]	NL[3]	NL[2]	NL[1]	NL[0]	gate_scan & display boundary	16'h003C
	R02h	W	1	X	X	X	X	X	X	INV[1]	INV[0]	X	X	X	X	X	X	X	X	inversion	16'h0000
	R03h	W	1	X	X	X	BGR	X	MDT[2]	MDT[1]	MDT[0]	X	X	ID[1]	ID[0]	X	X	X	X	GRAM access	16'h0030
	R04h	W	1	BLC_MIX	BLC_ON	SMLC_MODE	SMLC_ON		TR[1:0]		DIM	DBV[7:0]								SMLC & BLC	16'h2000
	R05h	W	1	X	X	X	X	X	X	X	X	X	X	X	X	PWM_DIV[2:0]				SMLC & BLC	16'h0000
	R06h	R	1	X	X	X	X	X	X	X	X	SMLC_DBV[7:0]								Backlight brightness @ SMLC_ON="H"	
	R07h	W	1	X	X	PT[1]	PT[0]	X	X	X	SPT	X	X	X	GON	CL	REV	D[1]	D[0]	partial,8-color, display ON	16'h0000
	R08h	W	1	X	X	X	X	FP[3]	FP[2]	FP[1]	FP[0]	X	X	X	X	BP[3]	BP[2]	BP[1]	BP[0]	Porch period	16'h0202
	R09h	R	1	X	X	X	X	X	X	X	X	SMLC_IMG_BR_LEVEL[7:0]								level of image brightness as a result of SMLC	
	R0Ah	W	1	X	X	X	X	X	OFC[2]	OFC[1]	OFC[0]	X	X	X	X	RTN[3]	RTN[2]	RTN[1]	RTN[0]	osc control & clock number per 1H	16'h0000
	R0Bh	W	1	X	X	X	X	X	X	X	RM	X	X	DM[1]	DM[0]	X	RIM[2]	RIM[1]	RIM[0]	interface & display clock	16'h0000
	R0Ch	W	1	X	SDT[2]	SDT[1]	SDT[0]	X	EQ[2]	EQ[1]	EQ[0]	X	GNO[2]	GNO[1]	GNO[0]	X	X	X	X	source and gate timing control	16'h0000
	R0Dh	W	1	X	X	X	X	X	X	X	X	X	X	SCN[5]	SCN[4]	SCN[3]	SCN[2]	SCN[1]	SCN[0]	gate scan position	16'h0000
	R0Eh	W	1	X	X	FLMI[1]	FLMI[0]	X	X	X		FLMP[8:0]								tearing effect prevention	16'h0000
	R0Fh	W	1	X	X	X	X	X	X	X	X	BLC_MIX_MIN[7:0]									16'h0000
Power Control System	R10h	W	1	X	X	X	X	X	X	X	X	DSTB	X	X	X	X	X	X	STB	standby	16'h0000
	R11h	W	1	X	X	X	X	X	BT[2]	BT[1]	BT[0]	X	X	X	X	X	SAP[2]	SAP[1]	SAP[0]		16'h0404
	R12h	W	1	X	X	APON	DPON		PON[3:0]			X	AON1	AON0	X	VC[3:0]					16'h0000
	R13h	W	1	X	X	X	X	X	X	DC3[1]	DC3[0]	X	X	DC2[1]	DC2[0]	X	X	DC1[1]	DC1[0]		16'h0000
	R14h	W	1	X	X	X	X	X	X	X	X	X	X	GVD[5:0]							16'h0000
	R15h	W	1	VML[7:0]							X	VMH_SEL	VMH[5:0]								16'h0000
	R16h	W	1	X	X	X	X	X	X	X	VCOMG	X	X	X	X	X	X	X	VCMR		16'h0100
	R18h	W	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	hidden	16'h0202
RAM Access Control	R20h	W	1	X	X	X	X	X	X	X	AD[17]	AD[16]	AD[15]	AD[14]	AD[13]	AD[12]	AD[11]	AD[10]	AD[9]	Y start address of GRAM	16'h0000
	R21h	W	1	X	X	X	X	X	X	X	AD[8]	AD[7]	AD[6]	AD[5]	AD[4]	AD[3]	AD[2]	AD[1]	AD[0]	X start address of GRAM	16'h0000
	R22h	W	1	WD[15]	WD[14]	WD[13]	WD[12]	WD[11]	WD[10]	WD[9]	WD[8]	WD[7]	WD[6]	WD[5]	WD[4]	WD[3]	WD[2]	WD[1]	WD[0]	write data to GRAM	x
	R22h	R	1	RD[15]	RD[14]	RD[13]	RD[12]	RD[11]	RD[10]	RD[9]	RD[8]	RD[7]	RD[6]	RD[5]	RD[4]	RD[3]	RD[2]	RD[1]	RD[0]	read data from GRAM	x
Gamma Control System	R28h	W	1	RPKP3[3:0]				RPKP2[3:0]				RPKP1[3:0]				RPKP0[3:0]				gamma	16'h8888
	R29h	W	1	X	X	X	X	X	X	X	X	RPKP5[3:0]				RPKP4[3:0]				gamma	16'h0088
	R2Ah	W	1	RPKN3[3:0]				RPKN2[3:0]				RPKN1[3:0]				RPKN0[3:0]				gamma	16'h8888
	R2Bh	W	1	X	X	X	X	X	X	X	X	RPKN5[3:0]				RPKN4[3:0]				gamma	16'h0088
	R2Ch	W	1	GPKP3[3:0]				GPKP2[3:0]				GPKP1[3:0]				GPKP0[3:0]				gamma	16'h8888
	R2Dh	W	1	X	X	X	X	X	X	X	X	GPKP5[3:0]				GPKP4[3:0]				gamma	16'h0088
	R2Eh	W	1	GPKN3[3:0]				GPKN2[3:0]				GPKN1[3:0]				GPKN0[3:0]				gamma	16'h8888
	R2Fh	W	1	X	X	X	X	X	X	X	X	GPKN5[3:0]				GPKN4[3:0]				gamma	16'h0088
	R30h	W	1	BPKP3[3:0]				BPKP2[3:0]				BPKP1[3:0]				BPKP0[3:0]				gamma	16'h8888
	R31h	W	1	X	X	X	X	X	X	X	X	BPKP5[3:0]				BPKP4[3:0]				gamma	16'h0088
	R32h	W	1	BPKN3[3:0]				BPKN2[3:0]				BPKN1[3:0]				BPKN0[3:0]				gamma	16'h8888
	R33h	W	1	X	X	X	X	X	X	X	X	BPKN5[3:0]				BPKN4[3:0]				gamma	16'h0088
	R34h	W	1	RPRN1[3:0]				RPRN0[3:0]				RPRP1[3:0]				RPRP0[3:0]				gamma	16'h8888
	R35h	W	1	GPRN1[3:0]				GPRN0[3:0]				GPRP1[3:0]				GPRP0[3:0]				gamma	16'h8888
	R36h	W	1	BPRN1[3:0]				BPRN0[3:0]				BPRP1[3:0]				BPRP0[3:0]				gamma	16'h8888
	R37h	W	1	X	X	X		RVRP1[4:0]				X	X	X		RVRP0[4:0]				gamma	16'h0000
	R38h	W	1	X	X	X	X	RVRN1[4:0]				X	X	X		RVRN0[4:0]				gamma	16'h0000
	R39h	W	1	X	X	X	X	GVRP1[4:0]				X	X	X		GVRP0[4:0]				gamma	16'h0000
	R3Ah	W	1	X	X	X		GVRN1[4:0]				X	X	X		GVRN0[4:0]				gamma	16'h0000
	R3Bh	W	1	X	X	X		BVRP1[4:0]				X	X	X		BVRP0[4:0]				gamma	16'h0000
	R3Ch	W	1	X	X	X		BVRN1[4:0]				X	X	X		BVRN0[4:0]				gamma	16'h0000
	R3Dh	W	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	SINGLE_ON	gamma	16'h0000

Table 7-2 : Instruction Table (to be continued)

	Reg. No	R/W	RS	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	description	default value
Position Control System	R40h	W	1	X	X	X	X	X	X	X	SS1[8]	SS1[7]	SS1[6]	SS1[5]	SS1[4]	SS1[3]	SS1[2]	SS1[1]	SS1[0]	1'st screen area(start)	16'h0000
	R41h	W	1	X	X	X	X	X	X	X	SE1[8]	SE1[7]	SE1[6]	SE1[5]	SE1[4]	SE1[3]	SE1[2]	SE1[1]	SE1[0]	1'st screen area(end)	16'h01DF
	R42h	W	1	X	X	X	X	X	X	X	SS2[8]	SS2[7]	SS2[6]	SS2[5]	SS2[4]	SS2[3]	SS2[2]	SS2[1]	SS2[0]	2'nd screen area(start)	16'h0000
	R43h	W	1	X	X	X	X	X	X	X	SE2[8]	SE2[7]	SE2[6]	SE2[5]	SE2[4]	SE2[3]	SE2[2]	SE2[1]	SE2[0]	2'nd screen area(end)	16'h0000
	R44h	W	1	X	X	X	X	X	X	X	HEA[8]	HEA[7]	HEA[6]	HEA[5]	HEA[4]	HEA[3]	HEA[2]	HEA[1]	HEA[0]	horizontal end ram address(window)	16'h013F
	R45h	W	1	X	X	X	X	X	X	X	HSA[8]	HSA[7]	HSA[6]	HSA[5]	HSA[4]	HSA[3]	HSA[2]	HSA[1]	HSA[0]	horizontal start ram address(window)	16'h0000
	R46h	W	1	X	X	X	X	X	X	X	VEA[8]	VEA[7]	VEA[6]	VEA[5]	VEA[4]	VEA[3]	VEA[2]	VEA[1]	VEA[0]	vertical end ram address(window)	16'h01DF
	R47h	W	1	X	X	X	X	X	X	X	VSA[8]	VSA[7]	VSA[6]	VSA[5]	VSA[4]	VSA[3]	VSA[2]	VSA[1]	VSA[0]	vertical sart ram address(window)	16'h0000
SMLC DBV	R48h	W	1	LV1_DBV[7:0]								LV2_DBV[7:0]								Brightness of Backlight for SMLC	16'h9199
	R49h	W	1	LV3_DBV[7:0]								LV4_DBV[7:0]								Brightness of Backlight for SMLC	16'h9BAA
	R4Ah	W	1	LV5_DBV[7:0]								LV6_DBV[7:0]								Brightness of Backlight for SMLC	16'hAAC1
	R4Bh	W	1	LV7_DBV[7:0]								LV8_DBV[7:0]								Brightness of Backlight for SMLC	16'hD5EE
ETC	R50h	W	1	X	X	OTM[1:0]		X	X	OTWE	OTRE	X	X	X	OTAD[4:0]					OTP	16'h0000
	R51h	W	1	X	X	X	X	X	X	OTWD[9:0]										OTP	16'h0000
	R52h	R	1	X	X	X	X	X	X	OTRD[9:0]										OTP	16'h0000
	R67h	W	1	X	X	X	X	TP_PASS	X	X	X	X	X	X	X	X	X	X	X	Test	16'h0800

INSTRUCTION DESCRIPTIONS

INDEX REGISTER

The index instruction specifies indexes. It can set the register address in the range of 00h to 7fh in hexadecimal form. However, do not access to index register and instruction bit that is not allocated.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	0	*	*	*	*	*	*	*	*	ADR7	ADR6	ADR5	ADR4	ADR3	ADR2	ADR1	ADR0

STATUS READ

The status read instruction reads the internal status. L[7:0] indicates the position of horizontal line being driven currently.

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	0	L7	L6	L5	L4	L3	L2	L1	L0	X	X	X	X	X	X	X	X

START OSCILLATION (R00h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	OSC_ON
R	1	0	1	1	1	0	1	1	0	0	0	0	0	0	0	0	1

OSC_ON : To set this register to “1” restarts the oscillator from the halt state in the standby mode.

OSC_ON = 1 : start oscillator

= 0 : stop oscillator

After issuing this instruction, wait at least 10ms for oscillation to stabilize before issuing the next instruction.

When STB register is set to “1”, this register is set to “0” automatically. However, this register should be set to “1” after STB register is set to “0”.

If this register is read forcibly, device code('h7601) is output.

DRIVER OUTPUT CONTROL (R01h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	VSPL	HSPL	DPL	EPL	X	SM	GS	0	X	X	NL[5:0]					

VSPL : Set the polarity of VSYNC input.

0 : Active low

1 : Active high

HSPL : Set the polarity of HSYNC input.

0 : Active low

1 : Active high

DPL : Set the polarity of DOTCLK input.

0 : data should be read at the rising edge of the DOTCLK

1 : data should be read at the falling edge of the DOTCLK

EPL : Set the polarity of ENABLE input

0 : Active low

1 : Active high

The following table shows the relationship between EPL, ENABLE, and DDRAM access.

Table 7-3 : DDRAM update with ENABLE & EPL

EPL	ENABLE	DDRAM write	DDRAM address
0	0	Valid	Updated
0	1	Invalid	Hold
1	0	Invalid	Hold
1	1	Valid	Updated

SM : Select the method of driving gate drivers. When SM=0 gate drivers are driven in Alternate scan mode, when SM=1 gate drivers are driven in Sequential scan mode (shown below).

GS : Set the shift direction of gate driver output. Enables setting the scan order in accordance with the scan mode adopted in the module.

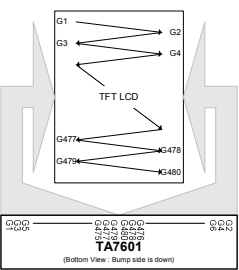
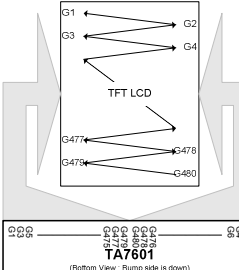
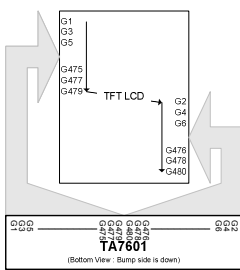
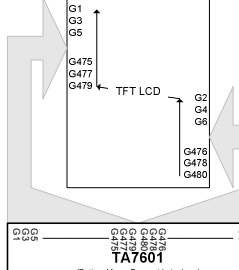
Scan mode	Alternate scan mode		Sequential scan mode	
Register	SM=0, GS=0	SM=0, GS=1	SM=1, GS=0	SM=1, GS=1
Shift direction of gate driver outputs				
	G1>G2>G3... ...G478>G479>G480	G480>G479>G478>... ...>G3>G2>G1	G1>G3>..G477>G479> G2>G4..G478>G480	G480>G478>..G4>G2> G479>G477..G3>G1

Figure 7-1 : Scan Direction Control (NL = 000000 & SCN = 000000)

When user sets NL to be 110010, scan direction is controlled as follows.

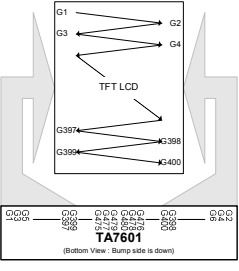
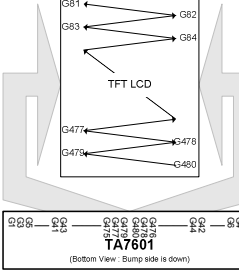
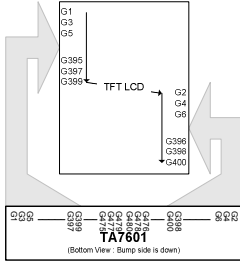
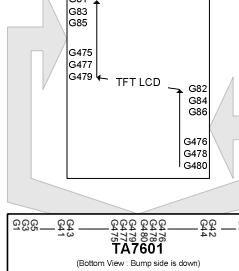
Scan mode	Alternate scan mode		Sequential scan mode	
Register	SM=0, GS=0	SM=0, GS=1	SM=1, GS=0	SM=1, GS=1
Shift direction of gate driver outputs				
	G1>G2>G3... ...G398>G399>G400	G480>G479>G478>... ...>G83>G82>G81	G1>G3>..G397>G399> G2>G4..G398>G400	G480>G478>..G84>G82> G479>G477..G83>G81

Figure 7-2 : Scan Direction Control (NL = 110010 & SCN = 000000)

NL[5:0] : Specify the number of horizontal lines to be driven. The number of the lines can be adjusted in units of eight. DDRAM address mapping is independent of this setting. The set value should be higher than the panel size.

Table 7-4 : NL Bits and Drive Duty

NL[5:0]	Display Size	Gate Driver – Lines Used
000000	Setting disabled	Setting disabled
000001	320-rgb X 8-line	G1 to G8
000010	320-rgb X 16-line	G1 to G16
----	----	----
101000	320-rgb X 320-line	G1 to G320
----	----	----
110010	320-rgb X 400-line	G1 to G400
----	----	----
111001	320-rgb X 456-line	G1 to G456
111010	320-rgb X 464-line	G1 to G464
111011	320-rgb X 472-line	G1 to G472
111100	320-rgb X 480-line	G1 to G480

[NOTE] An FP (front porch) and a BP (back porch) period will be inserted as blanking period before/after driving all gate lines.

LCD DRIVING WAVEFORM CONTROL (R02h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	INV[1:0]		X	X	X	X	X	X	X	X

INV[1:0] : Set LCD inversion method as shown below.

Table 7-5 : Inversion Control

INV[1:0]	Description
00	Frame Inversion
01	Mixed Inversion (Frame Inversion + Line Inversion)
10	No inversion. Active with positive polarity (VCOM = Low)
11	No inversion. Active with negative polarity (VCOM = High)

[NOTE] EQ function operates only in mixed inversion mode.

ENTRY MODE (R03h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	BGR	X	MDT[2:0]			X	X	ID[1:0]		X	X	X	X

BGR : When 18-bit data is written to DDRAM, RGB assignment can be controlled with this bit.

BGR = 0 : {DB[17:12],DB[11:6],DB[5:0]} is assigned to {R,G,B}.

= 1 : {DB[17:12],DB[11:6],DB[5:0]} is assigned to {B,G,R}.

MDT[2:0] : When user wants to transfer 260k color data on 8/16-bit parallel bus, MDT (Multiple Times Data Transfer) register may be used for that.

Table 7-6 : Multiple Times Data Transfer Mode Control

MDT[2:0]	IM[3:0]	Description
0XX	X	Normal Data Transfer. (See Logic IO Pins Description, Page 33)
100	0001 or 0011 (8-bit)	260k color data is transferred by 3 times Data Transfer
	0000 or 0010 (16-bit)	260k color data is transferred by 2 times Data Transfer
101	0001 or 0011 (8-bit)	65k color data is transferred by 3 times Data Transfer
	0000 or 0010 (16-bit)	260k color data is transferred by 2 times Data Transfer
11x	-	Setting disabled

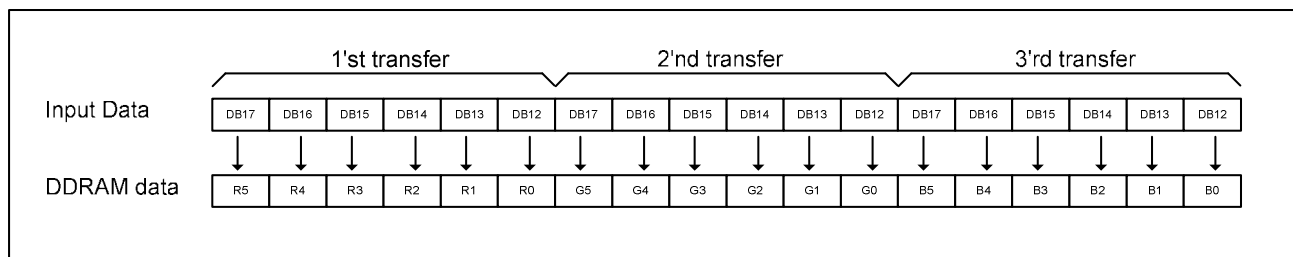


Figure 7-3 : 260k color data transfer on 8-bit parallel bus (MDT=3'b100)

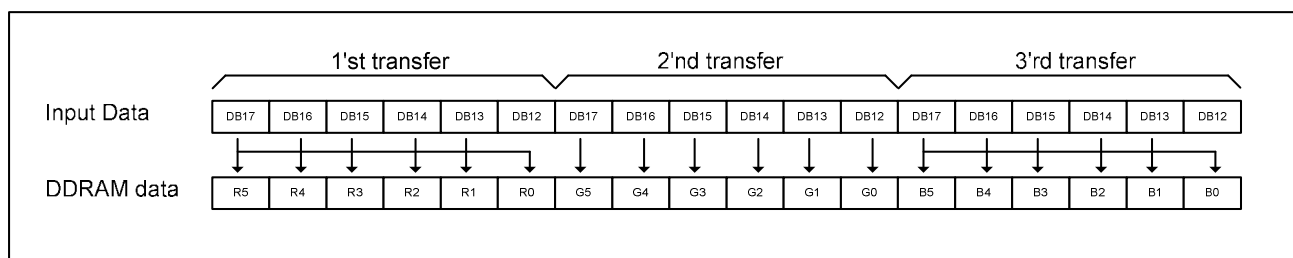


Figure 7-4 : 65k color data transfer on 8-bit parallel bus (MDT=3'b101)

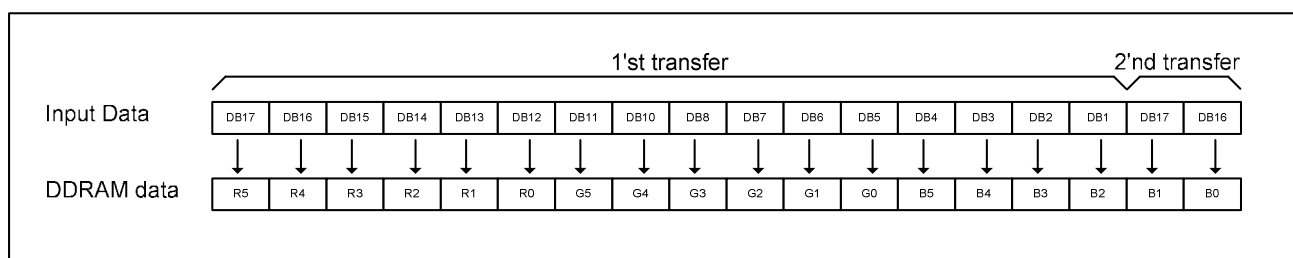


Figure 7-5 : 260k color data transfer on 16-bit parallel bus (MDT=3'b100)

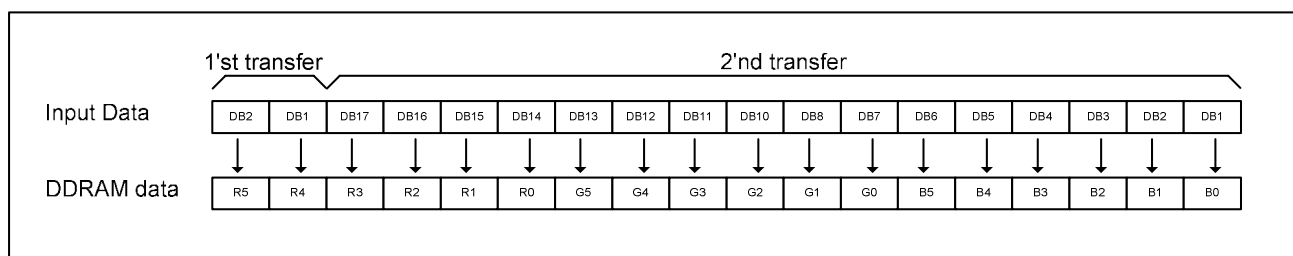
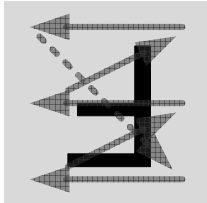
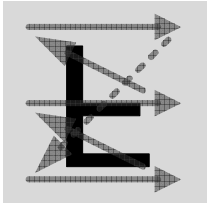
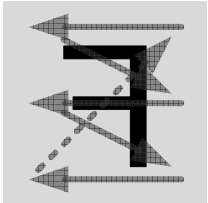
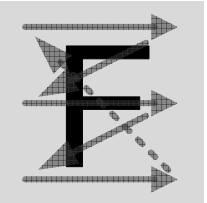


Figure 7-6 : 260k color data transfer on 16-bit parallel bus (MDT=3'b101)

[Note] The mapping direction between DDRAM and input data during the memory read operations is reversed.

ID[1:0] : When ID[1], ID[0] = 1, the internal address counter is automatically increased by 2 after the two consecutive data are written to the DDRAM. When ID[1], ID[0] = 0, the address counter is automatically decreased by 2 after the two consecutive data are written to the DDRAM. The increment/decrement setting of the address counter using ID[1:0] is done independently for the horizontal address and vertical address.

	ID[1:0] = "00" V : decrement H : decrement	ID[1:0] = "01" V : decrement H : increment	ID[1:0] = "10" V : increment H : decrement	ID[1:0] = "11" V : increment H : increment
Update Direction	<p>(000h, 000h)</p>  <p>(13Fh, 1DFh)</p>	<p>(13Fh, 000h)</p>  <p>(000h, 1DFh)</p>	<p>(13Fh, 000h)</p>  <p>(000h, 1DFh)</p>	<p>(000h, 000h)</p>  <p>(13Fh, 1DFh)</p>

[NOTE] Ensure that the starting addresses of written data are written within the window space.

When window addresses is set, the DDRAM can only be written within the window.

If you want to change source output direction, refer to Appendix.C for detail.

Figure 7-7 : Memory Update Direction Control

DISPLAY CONTROL (R04h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	BLC _MIX	BLC_ ON	SMLC_ MODE	SMLC_ ON	X	TR[1:0]		DIM	DBV[7:0]							

BLC_MIX :

1 : Final BLC duty is obtained based on SMLC_DBV multiplied by DBV.

0 : Final BLC duty is obtained DBV only or SMLC_DBV (according to SMLC_ON).

BLC_ON : Backlight control signal.

1 : Backlight becomes active and the brightness of Backlight is controlled by DBV[7:0] or the brightness of display image.

0 : Backlight becomes inactive

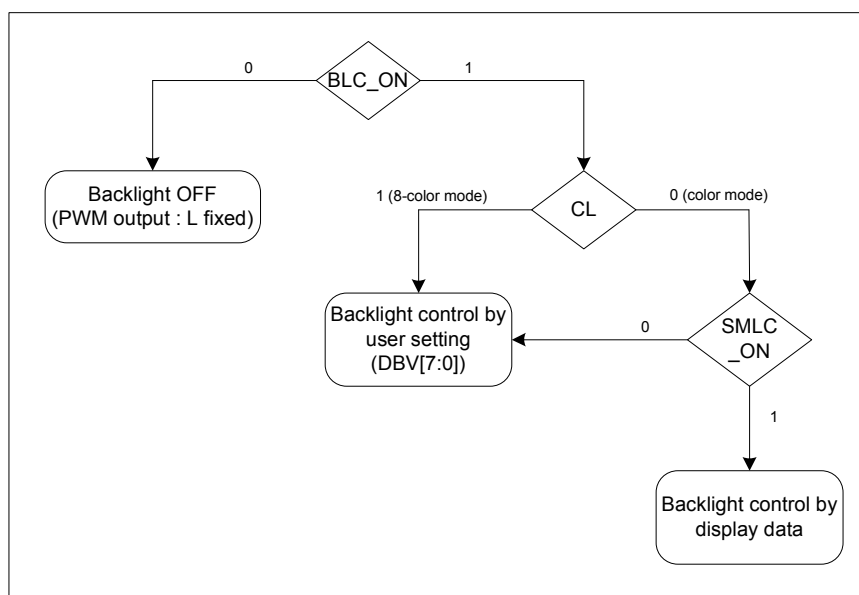


Figure 7-8 : Backlight Control Flow

SMLC_MODE : Selection higher power reduction or better image quality.

1 : lower power reduction and better image quality.

0 : higher power reduction and permitted a little image distortion.

SMLC_ON : SMLC(Smart Mobile Luminance Control) Function ON/OFF signal.

1 : BLC(PWM signal) is generated based on the display data analysis and luminance of display data is enhanced.

0 : BLC(PWM signal) is generated according to DBV register without any image enhancement.

TR[1:0] : When Dimming function is enabled, transition time is controlled using TR[1:0] as below.

Table 7-7 : Transition Time Control

TR[1:0]	Transition Time
2'b00	0-frame
2'b01	1-frame
2'b10	3-frame
2'b11	7-frame

[NOTE] When the brightness of input image changes abruptly frequently, it is recommended to use this Dimming Function to avoid flicker with the registers of TR and DIM.

DIM : Dimming function ON/OFF signal.

1 : Display dimming ON

0 : Display dimming OFF

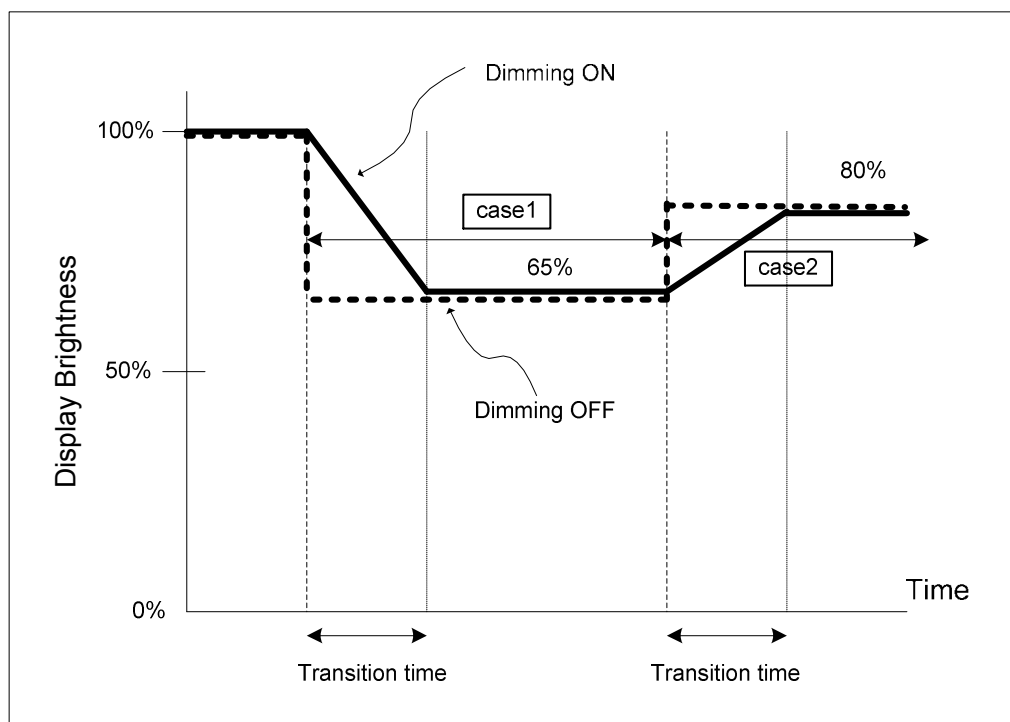


Figure 7-9 : Display Dimming Function

DBV[7:0] : This value is used to adjust the brightness of backlight. When SMLC_ON is set to "0", PWM signal (BLC) for backlight control is controlled by this register.

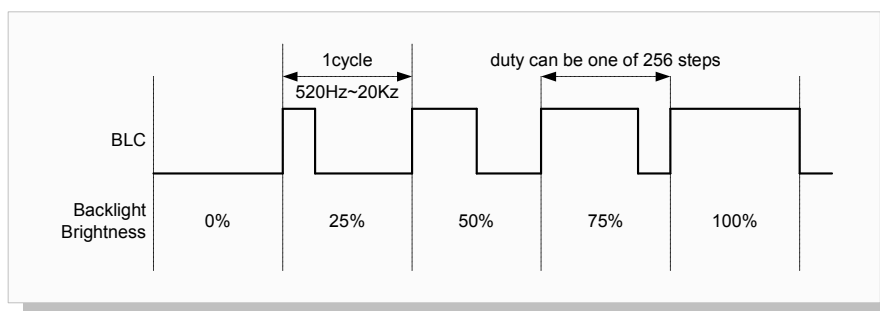


Figure 7-10 : The Period and Duty of PWM signal

DISPLAY CONTROL (R05h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1												PWM_DIV[2:0]				

PWM_DIV[2:0] : W-LED driver control signal (PWM) frequency control

Table : 7-1 : PWM Frequency Control

PWM_DIV[2:0]	PWM frequency	Remark (varies with OFC)
3'b000	(DISP_CK / 256)	8.40KHz ~ 20.00KHz
3'b001	(DISP_CK / 256) / 2	4.20KHz ~ 10.00KHz
3'b010	(DISP_CK / 256) / 4	2.10KHz ~ 5.00KHz
3'b011	(DISP_CK / 256) / 8	1.05KHz ~ 2.50KHz
3'b100	(DISP_CK / 256) / 16	0.52KHz ~ 1.250KHz
3'b101 ~ 3'b111	Setting disable	-

[NOTE] DISP_CK is internal signal which equals the internal oscillator clock or
DOTCLK divided by 4/8/12(based on RIM)

DISPLAY CONTROL (R06h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1									SMLC_DBV[7:0]							

SMLC_DBV[7:0] : Read-only Registers. When SMLC_ON register is set to “0”, SMLC_DBV value is not valid. SMLC_DBV is selected internally among R48h ~ R4Bh with relation to image processing. If you don't want to use the PWM signal (BLC) of this device, you can generate another PWM signal using this register value.

DISPLAY CONTROL (R07h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	PT[1:0]		X	X	X	SPT	X	X	X	GON	CL	REV	D[1:0]	

PT[1:0] : When the screen is partially displayed, these bits set the source output of non-display area. The partial display operation is shown below.

Table 7-8 : Non-Displayed Area Control

PT[1:0]	Source Output for Non-display area		Display Image	
	Positive Polarity	Negative Polarity	@normally Black Panel	@normally white Panel
00	V63 (Low Voltage)	V0 (High Voltage)	Black	White
01	V0	V63	White	Black
10	GND	GND	Black	White
11	Hi-z	Hi-z	-	-

[NOTE] GND means that Source level is equal to VCOM level.

SPT : When SPT = "1", the Partial Display Function is performed. For details, see "Partial Display Mode section" described later.

GON : gate ON/OFF control signal.

Table 7-9 : Gate Output Control

GON	Gate Output
0	Halt (VGL)
1	Normal operation (VGH / VGL)

CL : Select 8-color display mode. For details, see “8-color Display Mode section”.

We recommend SMLC_ON register should be “0” at 8-color mode.

Table 7-10 : Color Depth Control

CL	Color Depth
0	262,144 colors / 65,536 colors [NOTE]
1	8 colors

[NOTE] color depth is defined by IM[3:0] & MDT[2:0]

REV : Set REV=1 for a normally-white panel and REV=0 for a normally-black panel for correct display.

By setting REV=“1”, the grayscale of image can be inverted. This means, the REV allows both normally black and normally white panels to display same image with equal data. The source output level during non-display area in partial display mode is set with the PT[1:0].

Table 7-11 : Source Output Level Control

REV	DDRAM data	Source output level									
		Display Area		Non-display Area							
				PT[1:0] = “00”		PT[1:0] = “01”		PT[1:0] = “10”		PT[1:0] = “11”	
		Posi	Nega	Posi	Nega	Posi	Nega	Posi	Nega	Posi	Nega
0	6'h00	V63	V0	V63	V0	V0	V63	GND	GND	Hi-z	Hi-z
	~	~	~								
	6'h3F	V0	V63								
1	6'h00	V0	V63	V63	V0	V0	V63	GND	GND	Hi-z	Hi-z
	~	~	~								
	6'h3F	V63	V0								

[NOTE] GND means that Source level is equal to VCOM level.

D[1:0] : Specify source/VCOM output. For details, see the instruction Set-up Flow section.

Table 7-12 : Source/ VCOM Output Control

D [1:0]	Source Output	VCOM Output	Display Image	
			@normally Black Panel	@normally white Panel
00	GND	VCOML or VSSA [NOTE-1]	Black	White
01	GND	VCOML or VSSA [NOTE-1]	Black	White
10	GND	Normal operation	Black	White
11	Normal display	Normal operation	[DDRAM DATA]	[DDRAM DATA]

[NOTE]

1. Writing by host to the DDRAM is independent of D[1:0].
2. In standby mode, the D51E5TA7601 operates as D[1:0] = "00". However, the register of D is not modified.
3. In this table, GND means source drivers output are short to VCOM.

[NOTE-1]

When VCOMG is set to "1" VCOM Output becomes VSSA, otherwise VCOM Output becomes VCOML.

BLANK PERIOD CONTROL (R08h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	FP[3:0]				X	X	X	X	BP[3:0]			

FP[3:0]/BP[3:0] : Set the period of vertical blank period, which is placed at the beginning and the end of a frame. FP[3:0] is for a Front Porch control and BP[3:0] is for a Back Porch control. When Front Porch and Back Porch are set, the setting should meet the following conditions.

BP + FP <= 16 lines

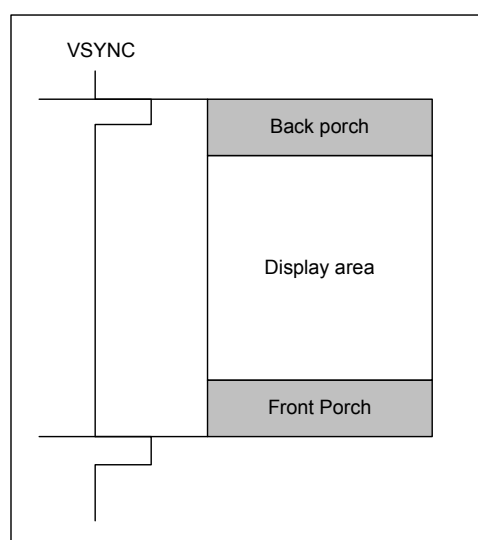
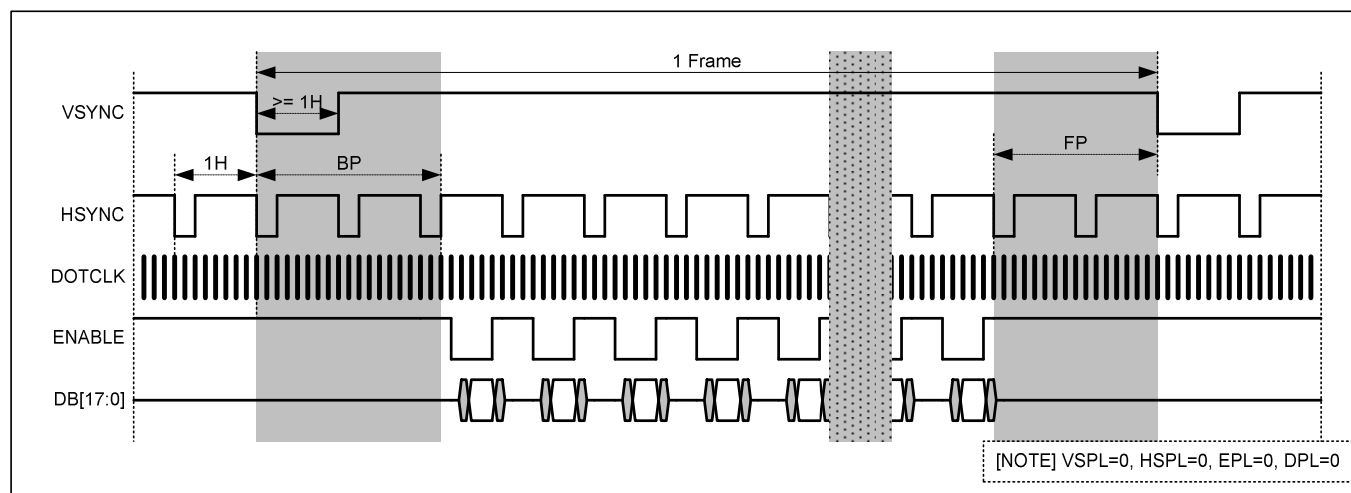
FP >= 2 lines

BP >= 2 lines

When the D51E5TA7601 operates in external clock operation mode, the BP will start on the falling (when VSPL = 0) edge of the VSYNC signal and display operation begins just after the Back Porch period. The FP will start when data of the number of lines specified by the NL has been displayed. During the period between the completion of the FP and the next VSYNC signal, the display will remain blank.

Table 7-13 : Blank Period Control with FP and BP

FP[3:0](BP[3:0])	Number of raster periods in Front(Back) Porch
0000	Setting disabled
0001	Setting disabled
0010	2
0011	3
0100	4
----	----
1000	8
----	----
1100	12
1101	13
1110	14
1111	Setting disabled



[NOTE] The output Timing to the LCD is delayed by 2-lines period from the input of synchronizing signal

Figure 7-11 : BP & FP in External Clock Operation Mode (DM[0] = "1")

DISPLAY CONTROL (R09h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	X	X	X	X	X	X	X	X	SMLC_IMG_BR_LEVEL[7:0]							

SMLC_IMG_BR_LEVEL[7:0] : TA7601 supports Backlight control function. There are two methods. One is manual control with DBV[7:0] register and the other is display image adaptive control with image enhancement (SMLC). TA7601 analyzes image, and then decides the level of image brightness. The brightness level of image can be one of 8 brightness level. Image 1st brightness level out of the previous 8 levels is dark, and image brightness becomes brighter going to 8th brightness level. We can know the level of image brightness by SMLC algorithm through SMLC_IMG_BR_LEVEL[7:0] registers. We can use this information when fine tuning of backlight brightness is necessary through LVx_DBV[7:0].

Table 7-14 : Image Brightness Control of SMLC

SMLC_IMG_BR_LEVEL[7:0]	Image Brightness
8'b10000000	Brightest
8'b01000000	Bright
---	---
8'b00000010	Dark
8'b00000001	Darkest

FRAME CYCLE CONTROL (R0Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	OFC[2:0]			X	X	X	X	RTN[3:0]			

OFC[2:0] : Select the oscillator frequency of internal oscillator

Table 7-15 : Oscillator Frequency Control (@ RTN[3:0]=0000)

OFC[2:0]	Internal operation clock frequency (Fosc, MHz) [To be finalized later]	Frame frequency(Hz)
000	5.12	120
001	4.70	110
010	4.25	100
011	3.85	90
100	3.40	80
101	3.00	70
110	2.60	60
111	2.15	50

[NOTE] Fosc = Internal oscillation frequency.

$$\text{Frame Frequency [Hz]} = \frac{F_{osc}}{\text{Clock Cycles per Raster Row X (Line Numbers + Blank Period)}}$$

Clock cycles per raster row ; RTN

Line numbers ; NL

Blank period ; Back Porch(BP) + Front Porch(FP)

RTN[3:0] : Sets 1H period

Table 7-16 : Clock Cycles per horizontal line

RTN[3:0]	Clock Cycles per horizontal line
0000	86 (DISP_CK)
0001	87 (DISP_CK)
----	----
1111	101 (DISP_CK)

[NOTE] DISP_CK is internal signal which equals the internal oscillator clock or DOTCLK divided by 4/8/12(based on RIM)

EXTERNAL DISPLAY INTERFACE CONTROL (R0Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	RM	X	X	DM[1:0]		X	RIM[2:0]		

RM : Specifies the interface for DDRAM access as shown below. This register and DM register can be set independently. The display data can be written through system interface by clearing this register while RGB interface is used.

Table 7-17 : RM and DDRAM Access

RM	DDRAM Access Interface
0	System interface
1	RGB interface

DM[1:0] : Specifies the display operation mode. The interface can be set based on the bits of DM[1:0]. In internal clock operation mode, the source clock for display operation comes from internal oscillator while in external clock operation mode, it comes from RGB interface

Table 7-18 : DM and Display operation mode

DM[1:0]	Display Operation Mode
00	Internal clock operation
01	External clock operation
10	Internal clock operation with VSYNC
11	Setting disable

RIM[2:0]: Specifies RGB interface mode and the division ratio to make a internal main clock (namely DISP_CLK) for external display operation. The division ratio is controlled by RIM as below.

Table 7-19 : External display mode and division ratio control to make DISP_CLK

RIM[2:0]	f(DISP_CLK)	RGB interface mode
000	-	Reserved
001	$f(\text{DOTCLK}) / 4$	18-bit RGB interface (1 transfer per pixel for 260k color)
010	$f(\text{DOTCLK}) / 4$	16-bit RGB interface (1 transfer per pixel for 65k color)
011	-	Reserved
100	-	Reserved
101	$f(\text{DOTCLK}) / 12$	6-bit RGB interface (3 transfer per pixel for 260k color)
110, 111	-	Reserved

LCD INTERFACE CONTROL (R0Ch)

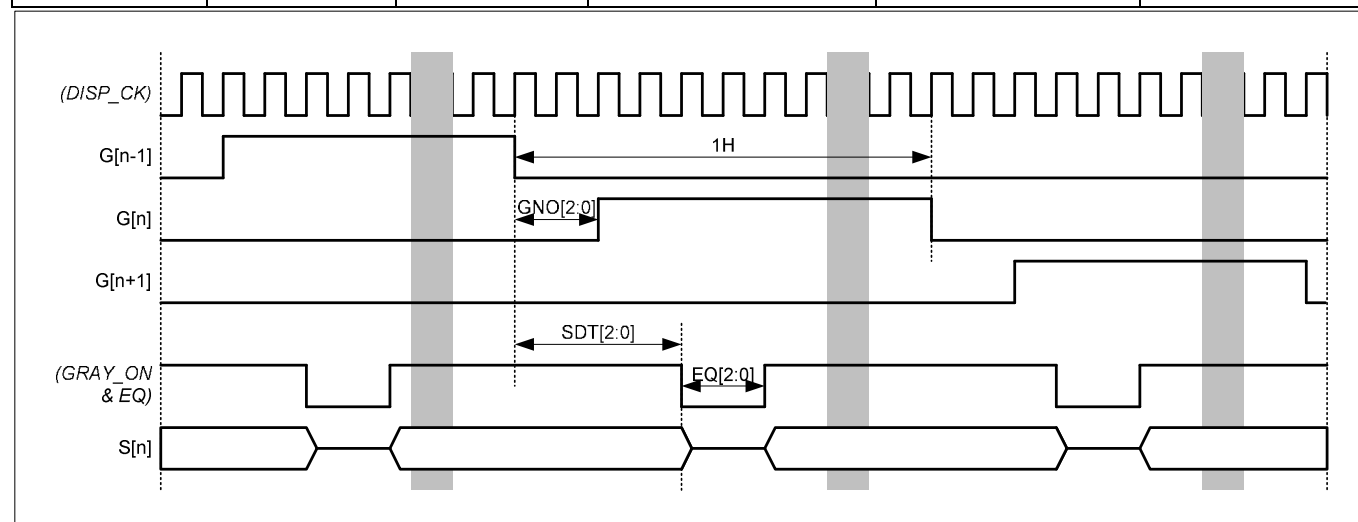
R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	SDT[2:0]			X	EQ[2:0]			X	GON[2:0]			X	X	X	X

The D51E5TA7601 outputs timing signals for controlling with built-in gates.

SDT[2:0]: Specifies the delay time from the starting point of 1H period(~ falling edge of the previous gate clock) to source output.

Table 7-20 : Source Output Delay Control

SDT[2:0]	Source output delay				
	DISP_CK	Internal Mode	External Mode		
		OSC	DOTCLK(@18/16-bit)	DOTCLK(@16-bit)	DOTCLK(@8/6-bit)
000	1-clock	1-clock	4-clock	8-clock	12-clock
001	2-clock	2-clock	8-clock	16-clock	24-clock
010	3-clock	3-clock	12-clock	24-clock	36-clock
011	4-clock	4-clock	16-clock	32-clock	48-clock
100	5-clock	5-clock	20-clock	40-clock	60-clock
101	6-clock	6-clock	24-clock	48-clock	72-clock
110	7-clock	7-clock	28-clock	56-clock	84-clock
111	8-clock	8-clock	32-clock	64-clock	96-clock



[NOTE] DISP_CK, GRAY_ON and EQ are internal signals.

Figure 7-12 : Source and Gate Timing Control

EQ[2:0] : Specifies equalization period to save power.

Table 7-21 : Equalization Period Control

EQ[2:0]	Equalization Period				
	DISP_CK	Internal Mode	External Mode		
		OSC	DOTCLK(@18/16-bit)	DOTCLK(@16-bit)	DOTCLK(@8/6-bit)
000	No EQ	No EQ	No EQ	No EQ	No EQ
001	1-clock	1-clock	4-clock	8-clock	12-clock
010	2-clock	2-clock	8-clock	16-clock	24-clock
011	3-clock	3-clock	12-clock	24-clock	36-clock
100	4-clock	4-clock	16-clock	32-clock	48-clock
101	5-clock	5-clock	20-clock	40-clock	60-clock
110	6-clock	6-clock	24-clock	48-clock	72-clock
111	7-clock	7-clock	28-clock	56-clock	84-clock

GNO[2:0]: Specifies non-overlap period between the falling edge of a gate output and the rising edge of the next gate output.

Table 7-22 : Non-overlap period control

EQ[2:0]	Non-overlap Period				
	DISP_CK	Internal Mode	External Mode		
		OSC	DOTCLK(@18/16-bit)	DOTCLK(@16-bit)	DOTCLK(@8/6-bit)
000	2-clock	2-clock	4-clock	8-clock	12-clock
001	3-clock	3-clock	8-clock	16-clock	24-clock
010	4-clock	4-clock	12-clock	24-clock	36-clock
011	5-clock	5-clock	16-clock	32-clock	48-clock
100	6-clock	6-clock	20-clock	40-clock	60-clock
101	7-clock	7-clock	24-clock	48-clock	72-clock
110	8-clock	8-clock	28-clock	56-clock	84-clock
111	9-clock	9-clock	32-clock	64-clock	96-clock

GATE SCAN POSITION CONTROL (R0Dh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	X	X	X	SCN[5:0]					

SCN[5:0]: Specifies the gate scanning starting position of the gate driver

Table 7-23 : Gate Scan Start Position Control

SCN[5:0]	Gate Scan Start Position (NL = 00000)	
	GS = 0	GS = 1
000000	G1	G480
000001	G9	G472
000010	G17	G464
----	----	----
00101	G41	G440
----	----	----
111001	G447	G24
111010	G465	G16
111011	G473	G8

SCN[5:0]	Gate Scan Start Position (NL = 110010)	
	GS = 0	GS = 1
000000	G1	G480
000001	G9	G472
000010	G17	G464
----	----	----
00101	G41	G440
----	----	----
101111	G377	G104
110000	G385	G96
110001	G393	G88

[NOTE] Ensure that gate scan start position (SCN) + the number of LCD driver lines (NL) \leq 480 when GS=0, and that gate start position (SCN) – the number of LCD driver lines (NL) \geq 0 when GS=1.

Frame Signal Control (R0Eh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	FLMI[1:0]		X	X	X	FLMP[8:0]								

FLMP[8:0]: Specifies the position of frame synchronization signal (FLM). A positive pulse is output some period (defined by this register) after internal frame synchronization signal. This can be used in image data writing operation for frame synchronization to avoid tearing effect.

Table 7-24 : The position of FLM

FLMP[8:0]	Position
9'h001	1
9'h002	2
---	---
9'h1E5	485
9'h1E6	486
9'h1E7	487

[NOTE] $9'h000 < FLMP \leq NL + BP + FP - 1$

FLMI[1:0]: Specifies the interval of frame synchronization signal (FLM) as shown below.

Table 7-25 : The interval of FLM

FLMI[1:0]	Interval
00	1 frame
01	2 frames
10	4 frames
11	6 frames

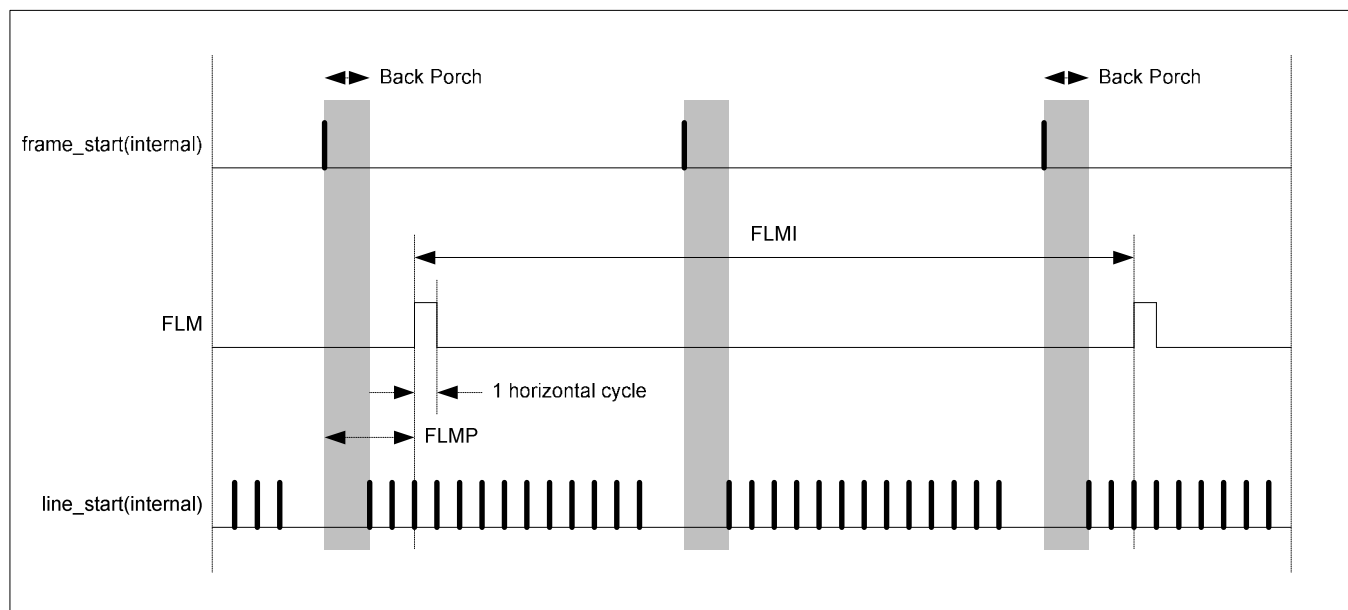


Figure 7-13 : FLM generation to prevent Tearing Effect on internal clock operation mode

DISPLAY CONTROL (R0Fh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1									BLC_MIX_MIN[7:0]							

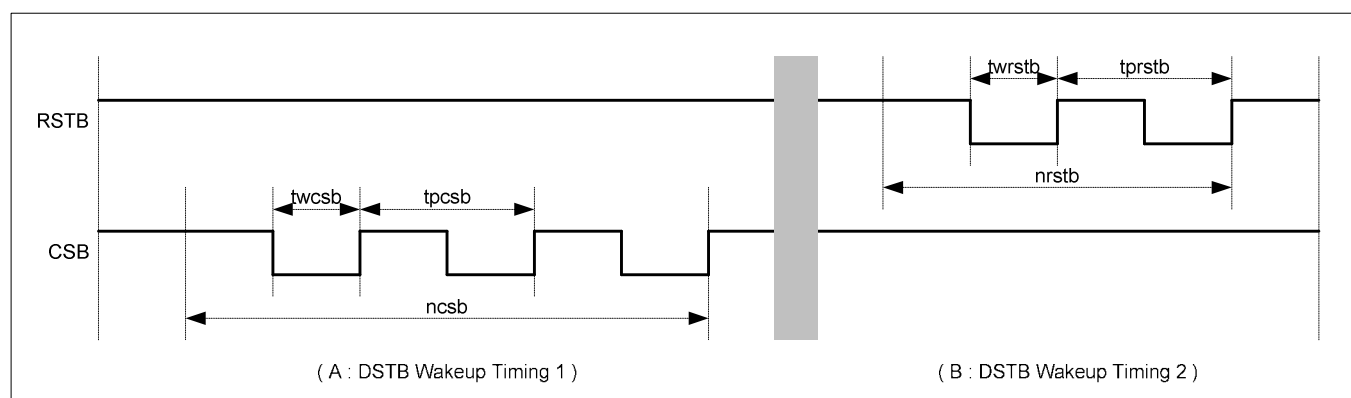
BLC_MIX_MIN[7:0] : Limits lowest value of backlight brightness when BLC_MIX is set to "1". Even if the SMLC_DBV multiplied by DBV is lower than MIN_BRIGHTNESS, the duty of BLC output signal cannot be smaller than MIN_BRIGHTNESS.

POWER CONTROL1 (R10h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	DSTB	X	X	X	X	X	X	X	STB

DSTB : Setting DSTB to 1 makes D51E5TA7601 enter deep standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator and RVDD. Further, any input signal except RSTB and CSB is ignored in this mode. For details, see Standby-In sequence and Deep Standby-In sequence. Any instructions can not be executed during in this mode.

To wake up this LSI in Deep Stand-by mode, host may assert RSTB or CSB like below.



Parameter	Description	Min	Max	Unit
twcsb	csb wakeup pulse width LOW	10	-	us
tpcsb	csb wakeup pulse period	20	-	us
ncsb	number of csb wakeup pulses(tpcsb)	2	-	ea
twrstb	rstb wakeup pulse width LOW	10	-	us
tprstb	rstb wakeup pulse period	20	-	us
nrstb	number of rstb wakeup pulses(tprstb)	1	-	ea

Figure 7-14 : Deep Stand-by Wake-Up Sequence

STB : Setting STB to 1 makes D51E5TA7601 enter the standby mode, where display operation completely stops, halting all the internal operations including the internal R-C oscillator. Further, no external clock pulses are supplied. For details, see the Standby Mode section. Only the following instructions can be executed during the standby mode.

- Standby mode cancel (STB = "0")
- Start oscillation (OSC_ON = "1")

Table 7-26 : Operation Modes for power save

Mode	Operation	Oscillator	RVDD
Normal	Active	Active	Active
Standby	Inactive	Inactive	Active
Deep Standby	Inactive	Inactive	Inactive

Power Control 2 (R11h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	x	x	x	x	x	BT[2:0]			x	x	x	x	x	SAP[2:0]		

BT[2:0] : Control of the boosting factor VGH/VGL generation.

BT[2:0]			Boosting Factor	
BT2	BT1	BT0	VGH	VGL
0	0	0	VCI1 X 6	VCI1 X – 5
0	0	1	VCI1 X 6	VCI1 X – 4
0	1	0	VCI1 X 6	VCI1 X – 3
0	1	1	VCI1 X 5	VCI1 X – 5
1	0	0	VCI1 X 5	VCI1 X – 4
1	0	1	VCI1 X 5	VCI1 X – 3
1	1	0	VCI1 X 4	VCI1 X – 4
1	1	1	VCI1 X 7	VCI1 X – 4

[NOTE] The values in the upper table mean upper-limit by register setting.

SAP[2:0] : Source driver output slew rate control. But faster operation consumes large current.

SAP2	SAP1	SAP0	Slew Rate of Op AMP for Source Driver
0	0	0	Source Amp off
0	0	1	Slow
0	1	0	Medium Slow1
0	1	1	Medium Slow2
1	0	0	Medium
1	0	1	Medium Fast1
1	1	0	Medium Fast2
1	1	1	Fast

Power Control 3 (R12h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	x	APON	DPON	PON0	x	PON3	PON2	PON1	x	AON[1:0]	x	VC[3:0]				

APON : This is an auto-operation-starting bit for the booster circuits. When APON=0, the auto booster sequence circuit is stopped, but the booster circuits are independently operated by PON0, PON1, PON2 and PON3 bits. In case of APON=1, booster circuits are automatically and sequentially operated. For further information about timing, please refer to the SET UP FLOW OF POWER SUPPLY.

DPON : This is an operation-starting bit for the dual step-up circuit1 (AVDD)

PON0 : This is an operation-starting bit for the step-up circuit1 (AVDD).

PON3 : This is an operation-starting bit for the step-up circuit3 (VCL).

PON2 : This is an operation-starting bit for the step-up circuit2 (VGL).

PON1 : This is an operation-starting bit for the step-up circuit2 (VGH).

AON[1:0] : This is an operation-starting bit for the Amplifiers.

Register Value		Regulator Control				
AON1	AON0	VREFO	VCI1	GVDD	VCOMH	VCOML
0	0	OFF	OFF	OFF	OFF	OFF
0	1	ON	OFF	OFF	OFF	OFF
1	0	ON	ON	OFF	OFF	OFF
1	1	ON	ON	ON	ON	ON

VC[3:0] : Set the VCI1 voltage. These bits control VCI1 voltage up to 3.0V as the normal output.
(upper limit value may depend on VCI voltage)

VC[3:0]	VCI1 (V)
0000	3
0001	2.9
0010	2.8
0011	2.76
0100	2.7
0101	2.66
0110	2.6
0111	2.56
1000	2.5
1001	2.4
1010	2.3
1011	2.2
1100	2.1
1101	1.9
1110	1.5
1111	VCI1=VCI

[NOTE] Don't set any VCI1 level higher than VCI

Power control 4 (R13h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	x	x	x	x	X	X	DC3[1:0]		X	X	DC2[1:0]		X	x	DC1[1:0]	

DC3[1:0] : Operating frequency in the Step-up circuit3 for the DC/DC converter.

DC3[1:0]	Frequency of Step-up circuit3 clock (DCCLK3)
00	Line Frequency * 4
01	Line Frequency * 2
10	Line Frequency * 1
11	Line Frequency * 0.5

[NOTE] Line frequency ; 1 / (period of 1 horizontal line display)

DC2[1:0] : Operating frequency in the Step-up circuit2 for the DC/DC converter

DC2[1:0]	Frequency of Step-up circuit2 clock (DCCLK2)
00	Line Frequency * 2
01	Line Frequency * 1
10	Line Frequency * 0.5
11	Line Frequency * 0.25

DC1[1:0] : Operating frequency in the Step-up circuit1 for the DC/DC converter

DC1[1:0]	Frequency of Step-up circuit1 clock (DCCLK1)
00	Line Frequency * 4
01	Line Frequency * 2
10	Line Frequency * 1
11	Line Frequency * 0.5

Power Control 5 (R14h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	x	X	x	x	x	x	x	x	x	x	GVD[5:0]					

GVD[5:0] : Set the amplified factor of the GVDD voltage (the voltage for the Gamma voltage).

GVD[5:0]	GVDD	GVD[5:0]	GVDD	GVD[5:0]	GVDD	GVD[5:0]	GVDD
000000	5.000	010000	4.467	100000	3.933	110000	3.400
000001	4.967	010001	4.433	100001	3.900	110001	3.367
000010	4.933	010010	4.400	100010	3.867	110010	3.333
000011	4.900	010011	4.367	100011	3.833	110011	3.300
000100	4.867	010100	4.333	100100	3.800	110100	3.267
000101	4.833	010101	4.300	100101	3.767	110101	3.233
000110	4.800	010110	4.267	100110	3.733	110110	3.200
000111	4.767	010111	4.233	100111	3.700	110111	3.167
001000	4.733	011000	4.200	101000	3.667	111000	3.133
001001	4.700	011001	4.167	101001	3.633	111001	3.100
001010	4.667	011010	4.133	101010	3.600	111010	3.067
001011	4.633	011011	4.100	101011	3.567	111011	3.033
001100	4.600	011100	4.067	101100	3.533	111100	3.000
001101	4.567	011101	4.033	101101	3.500	111101	-
001110	4.533	011110	4.000	101110	3.467	111110	-
001111	4.500	011111	3.967	101111	3.433	111111	-

[NOTE] Don't set any GVDD level higher than AVDD-0.5

Power Control 6 (R15h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	VML[7:0]									VMH_ SELB	VMH[5:0]					

VMH_SELB: VMH value selection between OTP and register.

1'b0 – OTP value is selected.

1'b1 – Register(R15h[5:0]:VMH) is selected.

VMH[5:0] : Set the upper level of the VCOM (VCOMH)

VMH[5:0]	VCOMH	VMH[5:0]	VCOMH	VMH[5:0]	VCOMH	VMH[5:0]	VCOMH
000000	5.000	010000	4.467	100000	3.933	110000	3.400
000001	4.967	010001	4.433	100001	3.900	110001	3.367
000010	4.933	010010	4.400	100010	3.867	110010	3.333
000011	4.900	010011	4.367	100011	3.833	110011	3.300
000100	4.867	010100	4.333	100100	3.800	110100	3.267
000101	4.833	010101	4.300	100101	3.767	110101	3.233
000110	4.800	010110	4.267	100110	3.733	110110	3.200
000111	4.767	010111	4.233	100111	3.700	110111	3.167
001000	4.733	011000	4.200	101000	3.667	111000	3.133
001001	4.700	011001	4.167	101001	3.633	111001	3.100
001010	4.667	011010	4.133	101010	3.600	111010	3.067
001011	4.633	011011	4.100	101011	3.567	111011	3.033
001100	4.600	011100	4.067	101100	3.533	111100	3.000
001101	4.567	011101	4.033	101101	3.500	111101	-
001110	4.533	011110	4.000	101110	3.467	111110	-
001111	4.500	011111	3.967	101111	3.433	111111	-

[NOTE] Don't set any VCOMH level higher than AVDD-0.5

VML[7:0] : Set the amplitude of the VCOM voltage. VCOML is adjusted automatically by setting the amplitude of VCOM

VML[7:0]	VCOM	VML[7:0]	VCOM	VML[7:0]	VCOM	VML[7:0]	VCOM	VML[7:0]	VCOM
00000000	6.00	00100000	5.36	01000000	4.72	01100000	4.08	10000000	3.44
00000001	5.98	00100001	5.34	01000001	4.70	01100001	4.06	10000001	3.42
00000010	5.96	00100010	5.32	01000010	4.68	01100010	4.04	10000010	3.40
00000011	5.94	00100011	5.30	01000011	4.66	01100011	4.02	10000011	3.38
00000100	5.92	00100100	5.28	01000100	4.64	01100100	4.00	10000100	3.36
00000101	5.90	00100101	5.26	01000101	4.62	01100101	3.98	10000101	3.34
00000110	5.88	00100110	5.24	01000110	4.60	01100110	3.96	10000110	4.32
00000111	5.86	00100111	5.22	01000111	4.58	01100111	3.94	10000111	43.30
00001000	5.84	00101000	5.20	01001000	4.56	01101000	3.92	10001000	3.28
00001001	5.82	00101001	5.18	01001001	4.54	01101001	3.90	10001001	3.26
00001010	5.80	00101010	5.16	01001010	4.52	01101010	3.88	10001010	3.24
00001011	5.78	00101011	5.14	01001011	4.50	01101011	3.86	10001011	3.22
00001100	5.76	00101100	5.12	01001100	4.48	01101100	3.84	10001100	3.20
00001101	5.74	00101101	5.10	01001101	4.46	01101101	3.82	10001101	3.18
00001110	5.72	00101110	5.08	01001110	4.44	01101110	3.80	10001110	3.16
00001111	5.70	00101111	5.06	01001111	4.42	01101111	3.78	10001111	3.14
00010000	5.68	00110000	5.04	01010000	4.40	01110000	3.76	10010000	3.12
00010001	5.66	00110001	5.02	01010001	4.38	01110001	3.74	10010001	3.10
00010010	5.64	00110010	5.00	01010010	4.36	01110010	3.72	10010010	3.08
00010011	5.62	00110011	4.98	01010011	4.34	01110011	3.70	10010011	3.06
00010100	5.60	00110100	4.96	01010100	4.32	01110100	3.68	10010100	3.04
00010101	5.58	00110101	4.94	01010101	4.30	01110101	3.66	10010101	3.02
00010110	5.56	00110110	4.92	01010110	4.28	01110110	3.64	10010110	3.00
00010111	5.54	00110111	4.90	01010111	4.26	01110111	3.62	10010111	-
00011000	5.52	00111000	4.88	01011000	4.24	01111000	3.60	10011000	-
00011001	5.50	00111001	4.86	01011001	4.22	01111001	3.58	10011001	-
00011010	5.48	00111010	4.84	01011010	4.20	01111010	3.56	10011010	-
00011011	5.46	00111011	4.82	01011011	4.18	01111011	3.54	10011011	-
00011100	5.44	00111100	4.80	01011100	4.16	01111100	3.52	10011100	-
00011101	5.42	00111101	4.78	01011101	4.14	00111101	3.50	10011101	-
00011110	5.40	00111110	4.76	01011110	4.12	01111110	3.48	10011110	-
00011111	5.38	00111111	4.74	01011111	4.10	01111111	3.46	10011111	-

[NOTE] Available setting range of VCOML is from VCL+0.5 to 0V. The Amplitude of VCOM cannot exceed 6V.

Power Control 7 (R16h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	x	X	x	x	x	X	X	VCOMG	x	x	x	x	x	x	X	VCMR

VCOMG : When VCOMG="1", low level of VCOM signal is to be fixed at VSSA. Therefore, the amplitude of VCOM signal is determined as $|VCOMH - VSSA|$ regardless of VML setting. In this case, VCOML pin can be open or connected to GND, because VCOML amp is off and VCOML output is floated.

When VCOMG = "0", the amplitude of VCOM signal is determined as $|VCOMH - VCOML|$.

VCMR : In case of VCMR is LOW, VCOMH is adjusted by VMH5-0 register and VCOMR pin is used to monitor the input current of the AMP which output the VCOMH voltage. In case of VCMR is HIGH, VMH5-0 register is ignored and VCOMH voltage is adjusted by VCOMR voltage which is externally supplied. The relationship between VCOMH and VCOMR is given as $VCOMH = 2.5 \times VCOMR$.

DDRAM ADDRESS (R20h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	AD[17:9]								

DDRAM ADDRESS (R21h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	AD[8:0]								

AD[17:0] : You can write initial DDRAM address into internal Address Counter (AC). When DDRAM data is transferred through system interface or RGB interface, the AC is automatically updated according to ID. This allows consecutive write without re-setting address in AC.

Ensure that the address is set within the specified window area specified with VSA, VEA, HSA, and HEA.

When RGB interface is used (RM="1") to access DDRAM, AD[17:0] will be set in the AC at the starting (falling when VSPL=0) edge of the VSYNC signal. And when system interface is used (RM="0"), AD[17:0] will be set upon the execution of an instruction.

Table 7-27 : DDRAM Address and Display

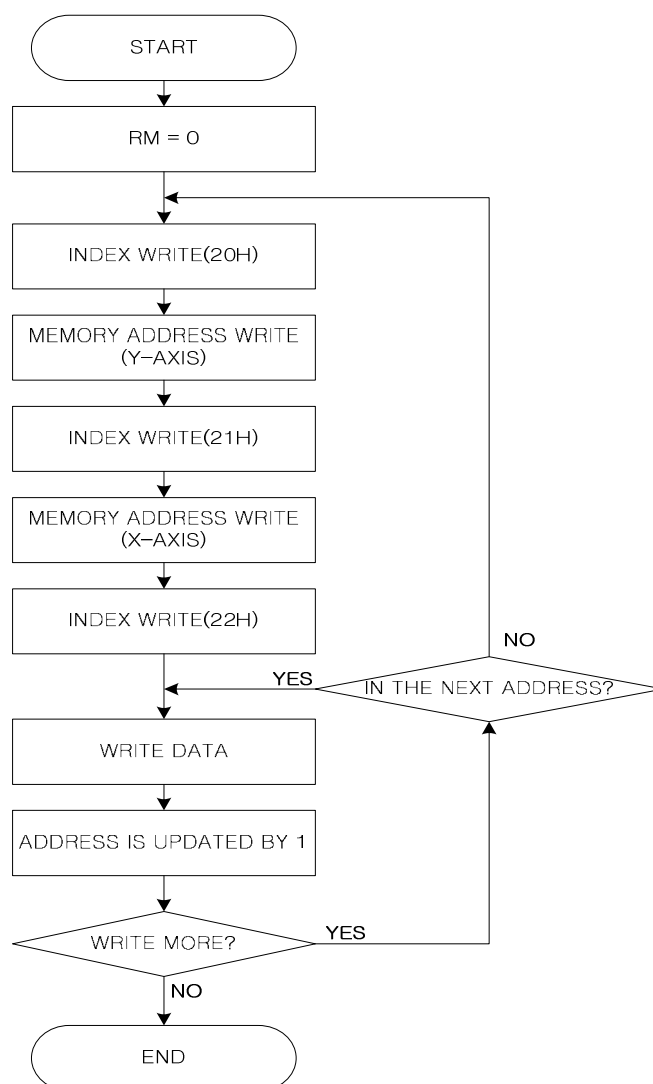
(AD[8:0], AD[17:9])	DDRAM setting
(000h, 000h) to (13Fh, 000h)	Bitmap data for G1
(000h, 001h) to (13Fh, 001h)	Bitmap data for G2
(000h, 002h) to (13Fh, 002h)	Bitmap data for G3
(000h, 003h) to (13Fh, 003h)	Bitmap data for G4
(000h, 1DCh) to (13Fh, 1DCh)	Bitmap data for G477
(000h, 1DDh) to (13Fh, 1DDh)	Bitmap data for G478
(000h, 1DEh) to (13Fh, 1DEh)	Bitmap data for G479
(000h, 1DFh) to (13Fh, 1DFh)	Bitmap data for G480

[NOTE] AD[17:9] : row address, AD[8:0] : column address

WRITE DATA TO DDRAM (R22h)

WDR : Data on DB bus is expanded to 18-bit before being written to DDRAM and the data determines grayscale level of source output. Please keep in mind that the expansion format varies with interface mode.

DDRAM can not be accessed in Standby mode. When data is written to DDRAM being used by RGB interface via the system interface, please make sure that write data conflicts do not occur.

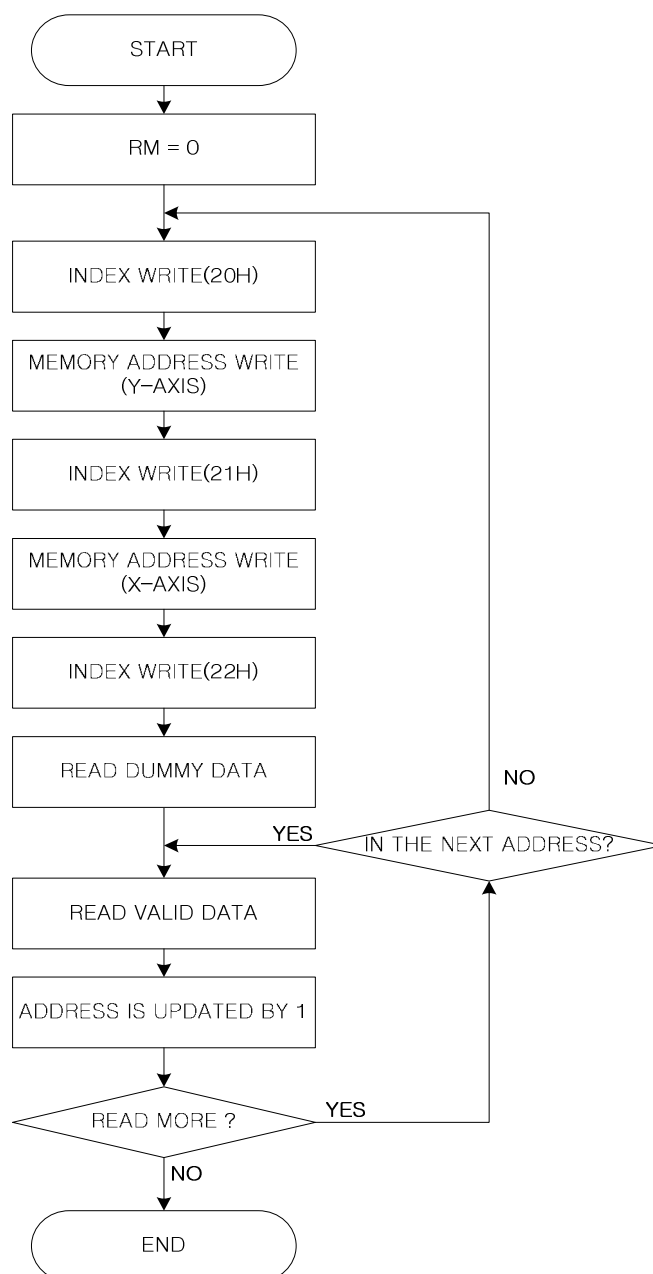


[NOTE] It is required that y-address (R20h) should be set before setting x-address (R21h).

Figure 7-15 : Memory Data Write Sequence

READ DATA FROM DDRAM (R22h)

RDR : You may read data from DDRAM using this register. When you make read operations, you can get a proper data on the second read operation as shown below. The first word you get just after address setting may be invalid.



[NOTE] It is required that y-address (R20h) should be set before setting x-address (R21h).

Figure 7-16 : Memory Data Read Sequence

. GAMMA CONTROL (R28h-R3Ch)

	R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R28h	W	1	RPKP3[3:0]				RPKP2[3:0]				RPKP1[3:0]				RPKP0[3:0]			
R29h	W	1	X	X	X	X	X	X	X	X	RPKP5[3:0]				RPKP4[3:0]			
R2Ah	W	1	RPKN3[3:0]				RPKN2[3:0]				RPKN1[3:0]				RPKN0[3:0]			
R2Bh	W	1	X	X	X	X	X	X	X	X	RPKN5[3:0]				RPKN4[3:0]			
R2Ch	W	1	GPKP3[3:0]				GPKP2[3:0]				GPKP1[3:0]				GPKP0[3:0]			
R2Dh	W	1	X	X	X	X	X	X	X	X	GPKP5[3:0]				GPKP4[3:0]			
R2Eh	W	1	GPKN3[3:0]				GPKN2[3:0]				GPKN1[3:0]				GPKN0[3:0]			
R2Fh	W	1	X	X	X	X	X	X	X	X	GPKN5[3:0]				GPKN4[3:0]			
R30h	W	1	BPKP3[3:0]				BPKP2[3:0]				BPKP1[3:0]				BPKP0[3:0]			
R31h	W	1	X	X	X	X	X	X	X	X	BPKP5[3:0]				BPKP4[3:0]			
R32h	W	1	BPKN3[3:0]				BPKN2[3:0]				BPKN1[3:0]				BPKN0[3:0]			
R33h	W	1	X	X	X	X	X	X	X	X	BPKN5[3:0]				BPKN4[3:0]			
R34h	W	1	RPRN1[3:0]				RPRN0[3:0]				RPRP1[3:0]				RPRP0[3:0]			
R35h	W	1	GPRN1[3:0]				GPRN0[3:0]				GPRP1[3:0]				GPRP0[3:0]			
R36h	W	1	BPRN1[3:0]				BPRN0[3:0]				BPRP1[3:0]				BPRP0[3:0]			
R37h	W	1	X	X	X	RVRP1[4:0]					X	X	X	RVRP0[4:0]				
R38h	W	1	X	X	X	RVRN1[4:0]					X	X	X	RVRN0[4:0]				
R39h	W	1	X	X	X	GVRP1[4:0]					X	X	X	GVRP0[4:0]				
R3Ah	W	1	X	X	X	GVRN1[4:0]					X	X	X	GVRN0[4:0]				
R3Bh	W	1	X	X	X	BVRP1[4:0]					X	X	X	BVRP0[4:0]				
R3Ch	W	1	X	X	X	BVRN1[4:0]					X	X	X	BVRN0[4:0]				

RPKP5-0[3:0]: Gamma fine adjusting register for Red sub-pixel on positive polarity

RPKN5-0[3:0]: Gamma fine adjusting register for Red sub-pixel on negative polarity

GPKP5-0[3:0]: Gamma fine adjusting register for Green sub-pixel on positive polarity

GPKN5-0[3:0]: Gamma fine adjusting register for Green sub-pixel on negative polarity

BPKP5-0[3:0]: Gamma fine adjusting register for Blue sub-pixel on positive polarity

BPKN5-0[3:0]: Gamma fine adjusting register for Blue sub-pixel on negative polarity

RPRP1-0[3:0]: Gamma gradient adjusting register for Red sub-pixel on positive polarity

RPRN1-0[3:0]: Gamma gradient adjusting register for Red sub-pixel on negative polarity

GPRP1-0[3:0]: Gamma gradient adjusting register for Green sub-pixel on positive polarity

GPRN1-0[3:0]: Gamma gradient adjusting register for Green sub-pixel on negative polarity

BPRP1-0[3:0]: Gamma gradient adjusting register for Blue sub-pixel on positive polarity

BPRN1-0[3:0]: Gamma gradient adjusting register for Blue sub-pixel on negative polarity

RVRP01-0[4:0]: Gamma amplitude adjusting register for Red sub-pixel on positive polarity

RVRN01-0[4:0]: Gamma amplitude adjusting register for Red sub-pixel on negative polarity

GVRP01-0[4:0]: Gamma amplitude adjusting register for Green sub-pixel on positive polarity

GVRN01-0[4:0]: Gamma amplitude adjusting register for Green sub-pixel on negative polarity

BVRP01-0[4:0]: Gamma amplitude adjusting register for Blue sub-pixel on positive polarity

BVRN01-0[4:0]: Gamma amplitude adjusting register for Blue sub-pixel on negative polarity

Partial (SPLIT) SCREEN1 DRIVING CONTROL (R40h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	SS18	SS17	SS16	SS15	SS14	SS13	SS12	SS11	SS10

Partial (SPLIT) SCREEN1 DRIVING CONTROL (R41h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	SE18	SE17	SE16	SE15	SE14	SE13	SE12	SE11	SE10

Partial (SPLIT) SCREEN2 DRIVING CONTROL (R42h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	SS28	SS27	SS26	SS25	SS24	SS23	SS22	SS21	SS20

Partial (SPLIT) SCREEN2 DRIVING CONTROL (R43h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	SE28	SE27	SE26	SE25	SE24	SE23	SE22	SE21	SE20

SS1[8:0] : Specifies the start position of the 1'st screen to drive in a line unit. The LCD display starts from "SS1 + 1".

SE1[8:0] : Specifies the end position of the 1'st screen to drive in a line unit. The LCD display is performed to the "SE1 + 1". For instance, when SS1[7:0] = "007h" and SE1[7:0] = "010h" are set, the LCD display is performed from G8 to G17, and white or black display is performed according to PT for G1 to G7, G18 and others. Ensure that SS1[7:0] <= SE1[7:0] <= "1DFh".
For details, see "Partial Display Mode".

SS2[8:0] : Specifies the start position of the 2'nd screen to display in a line unit. The LCD display starts from "SS2 + 1".
The 2'nd screen is displayed when SPT = "1".

SE2[8:0] : Specifies the end position of the 2'nd screen to display in a line unit. The LCD display is performed to the "SE2 + 1". For instance, when SS2[7:0] = "020h" and SE2[7:0] = "04Fh" and SPT = "1" are set, the LCD display is performed from G33 to G80. Ensure that "000h" <= SS1[7:0] <= SE1[7:0] <= SS2[7:0] <= SE2[7:0] <= "1DFh".
For details, see "Partial Display Mode".

HORIZONTAL RAM ADDRESS POSITION (R44h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	HEA[8:0]								

HORIZONTAL RAM ADDRESS POSITION (R45h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	HSA[8:0]								

HSA[8:0], HEA[8:0] : Specifies the horizontal start/end position of a Window for access to the specified partial memory (Window). Data can be written to DDRAM from the address specified by HSA[8:0] to the address specified by HEA[8:0]. Note that the Window Address must be set before DDRAM is updated. Ensure "00h" <= HSA[8:0] <= HEA[8:0] <= "13Fh". Ensure $HSA[8:0] = 2n$, $HEA[8:0] = 2n+1$ ($n=0,1,2,\dots,159$).

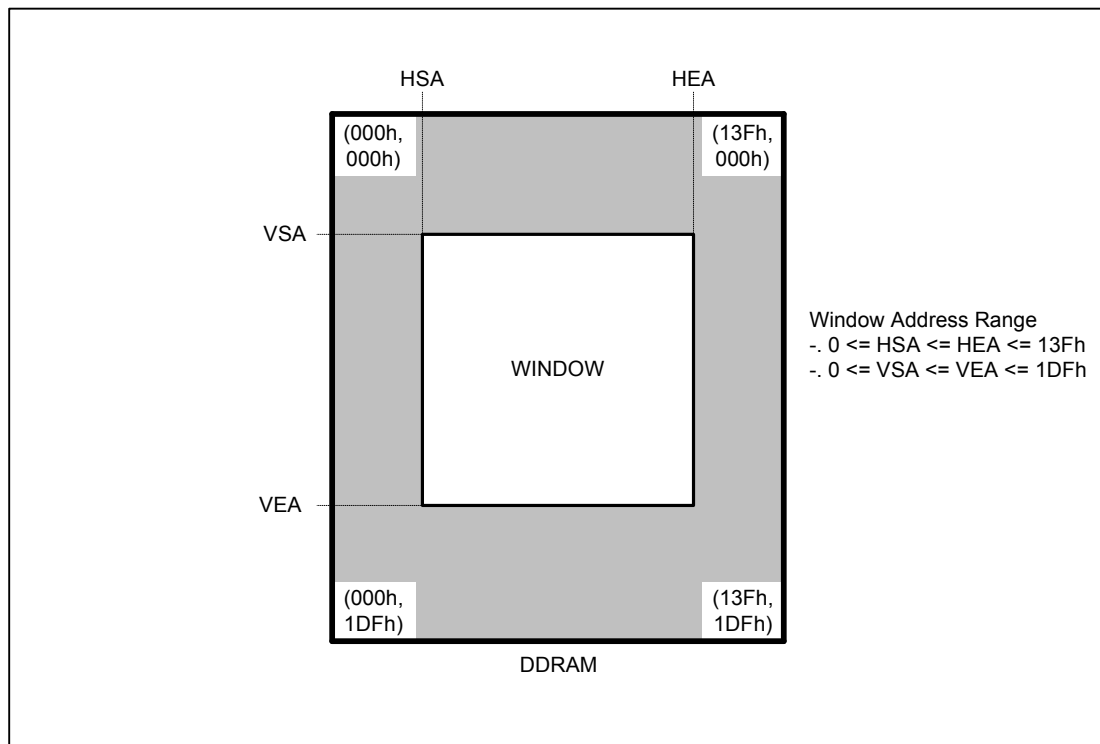
VERTICAL RAM ADDRESS POSITION (R46h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	VEA[8:0]								

VERTICAL RAM ADDRESS POSITION (R47h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	X	X	X	X	X	VSA[8:0]								

VSA[8:0], VEA[8:0] : Specifies the vertical start/end position of a Window for access to the specified partial memory (Window). Data can be written to DDRAM from the address specified by VSA[8:0] to the address specified by VEA[8:0]. Note that the Window Address must be set before DDRAM is updated. Ensure "000h" <= VSA[8:0] <= VEA[8:0] <= "1DFh".

**Figure 7-17 : Window Address Function**

[NOTE] Ensure that the Window addresses are within the DDRAM address space.

[NOTE] When the window area is changed, start the address (AD[8:0](R21) and AD[17:9](R20)) should be updated properly related to new window area

[NOTE] Horizontal size of the window should be even.

BACKLIGHT BRIGHTNESS ACCORDING TO THE LEVEL OF IMAGE BRIGHTNESS (R48h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	LV10_DBV[7:0]								LV11_DBV[7:0]							

LV1_DBV[7:0] : This is high pulse width of PWM signal for Backlight control when SMLC_IMG_BR_LEVEL is 8'b00000001.

LV2_DBV[7:0] : This is high pulse width of PWM signal for Backlight control when SMLC_IMG_BR_LEVEL is 8'b00000010.

BACKLIGHT BRIGHTNESS ACCORDING TO THE LEVEL OF IMAGE BRIGHTNESS (R49h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	LV2_DBV[7:0]								LV3_DBV[7:0]							

LV3_DBV[7:0] : This is high pulse width of PWM signal for Backlight control when SMLC_IMG_BR_LEVEL is 8'b00000100.

LV4_DBV[7:0] : This is high pulse width of PWM signal for Backlight control when SMLC_IMG_BR_LEVEL is 8'b00001000.

BACKLIGHT BRIGHTNESS ACCORDING TO THE LEVEL OF IMAGE BRIGHTNESS (R4Ah)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	LV4_DBV[7:0]								LV5_DBV[7:0]							

LV5_DBV[7:0] : This is high pulse width of PWM signal for Backlight control when SMLC_IMG_BR_LEVEL is 8'b00010000.

LV6_DBV[7:0] : This is high pulse width of PWM signal for Backlight control when SMLC_IMG_BR_LEVEL is 8'b00100000.

BACKLIGHT BRIGHTNESS ACCORDING TO THE LEVEL OF IMAGE BRIGHTNESS (R4Bh)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	LV4_DBV[7:0]								LV5_DBV[7:0]							

LV7_DBV[7:0] : This is high pulse width of PWM signal for Backlight control when SMLC_IMG_BR_LEVEL is 8'b01000000.

LV8_DBV[7:0] : This is high pulse width of PWM signal for Backlight control when SMLC_IMG_BR_LEVEL is 8'b10000000.

VCOM CONTROL1 (R50h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	OTM[1:0]		X	X	OTWE	OTRE	X	X	X	OTAD[4:0]				

OTM[1:0] : Multi-bit write control for VCOM programming.

Table 7-28 : VCOM Write Control

OTM[1:0]	Operation
2'b00	Ten bits are burnt serially one by one.
2'b01	5 bits are burnt simultaneously. So two internal write operations are done automatically.
2'b10	10 bits are burnt simultaneously.
2'b11	Reserved.

OTWE : OTP Write Enable

1 : Write operation

0 : NOP

OTRE : OTP Read Enable

1 : Read operation

0 : NOP

OTAD[4:0] : Read/Write address for OTP. The OTP value of the highest address among previously written address is actually used. So, user should use OTP cells from lowest address to 1 upper address in order to all 5 OTP cells.

Table 7-29 : OTP map

OTAD[4:0]	OTWD[9:3]	OTWD[2:0]
'd0	VCOM Set1	000
'd1	VCOM Set2	000
'd2	VCOM Set3	000
'd3	VCOM Set4	000
'd4	VCOM Set5	000

[NOTE] TA7601 provides multiple OTP (max. 5-times) that means user can write VCOM data to the OTP cells 5times max.

VCOM CONTROL2 (R51h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	X	X	x	X	X	X	OTWD[9:0]									

OTWD[9:0] : Write Data for VCOM setting, OTWD[9] is Header bit, OTWD[8:3] VCOM control data. In case of OTP programming for VCOM data, OTWD[9] is set to '1'.

OTP CONTROL3 (R52h)

R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
R	1	X	X	x	X	X	X	OTRD[9:0]									

OTRD[9:0] : Read Data When OTRE is high.

CABC Control (R67h)

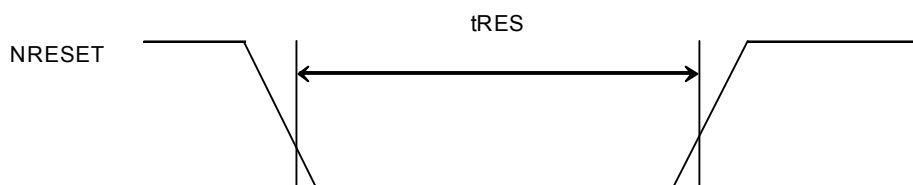
R/W	RS	IB15	IB14	IB13	IB12	IB11	IB10	IB9	IB8	IB7	IB6	IB5	IB4	IB3	IB2	IB1	IB0
W	1	0	0	0	0	TP_ PASS	0	1	0	0	0	0	0	0	0	0	0

TP_PASS : tests power consumption reduction for some test patterns(Red, Green, Blue).

“1” – by-pass the test patterns without any enhancement.

“0” – enhance the test patterns for power consumption reduction.

8. Reset Function



[NOTE] Does not guarantee reset operation due to the pulse of which width is between 0.5us and 2.0us.

Figure 8-1 : Reset Pulse Timing

Item	Symbol	Condition	Min	Typ	Max	Unit
Reset Low Pulse width	tRES		10	-	-	us

[NOTE] IOVCI: 2.8V, VCI =2.8V, TA=25 degrees C

9. Internal Power Supply

D51E5TA7601 has internal power supply output circuit to drive TFT panel. Please set up each voltage according to the LCD panel.

9.1. Internal Power Supply Circuit

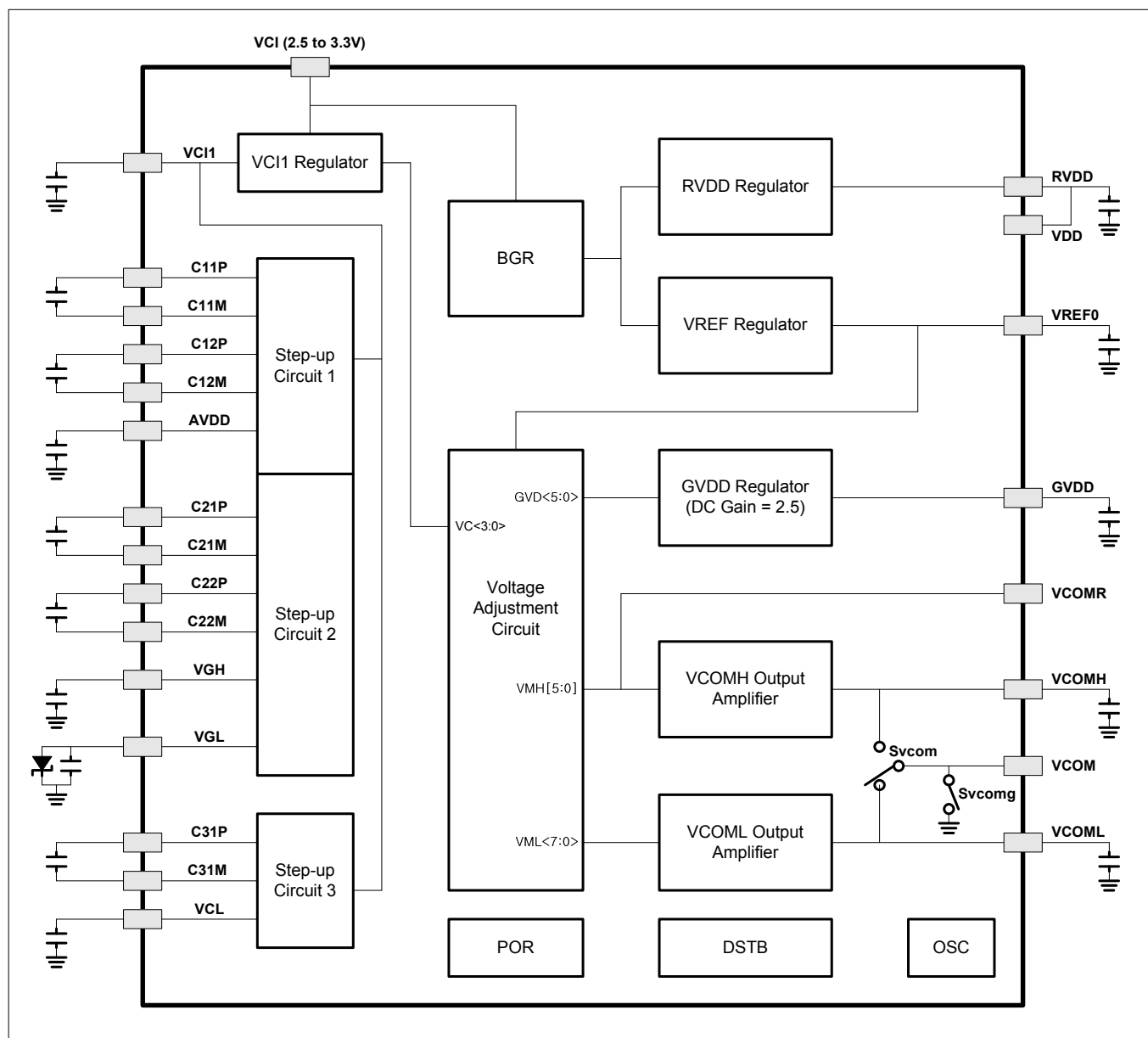


Figure 9-1 : Internal Power Supply Circuit

9.2. Internal Power Description

Table 9-1 : Internal Power Description

Name	Description	Range	Note
RVDD	Logic power supply	Typ 1.5V	
VREFO	Reference voltage for VCI1, GVDD, VCOMH/L	Typ 2.0V	
GVDD	The source driver grayscale and VCOM reference voltage	Refer to the description of the registers (GVD[5:0])	The following conditions must be met: $3V \leq GVDD \leq AVDD - 0.5V$
VCI1	Reference voltage for the step-up circuit 1, 2 and 3	Refer to the description of the registers (VC[3:0])	The following conditions must be met: 1.7 to 3.0V
AVDD	Output of the step-up circuit 1	$VCI1 \times 2$	Power supply for GVDD/Source/VCOM Block. Do not exceed 5.5V.
VGH	Gate on voltage	$VCI1 \times 7$ $VCI1 \times 6$ $VCI1 \times 5$ $VCI1 \times 4$	VGL is determined by BT[2:0] register setting Do not exceed 19.25V. Connect capacitor for stabilization on FPC.
VGL	Gate off voltage (Low)	$VCI1 \times (-5)$ $VCI1 \times (-4)$ $VCI1 \times (-3)$	VGL is determined by BT[2:0] register setting (Required to keep VGL higher than -13.75V.)
VCL	Output of the step-up circuit 3	$VCI1 \times (-1)$	Power supply for the VCOML circuit
VCOML	VCOM voltage (Low)	Refer to the description of the R15h registers (VMH[5:0], VML[7:0])	The following conditions must be met: $VCL + 0.5V \leq VCOML \leq 0V$.
VCOMH	VCOM voltage (High)		The following conditions must be met: $3V \leq VCOMH \leq AVDD - 0.5V$
VCOM	VCOM voltage		Outputs VCOMH and VCOML alternately

9.3. Internal Power Generation

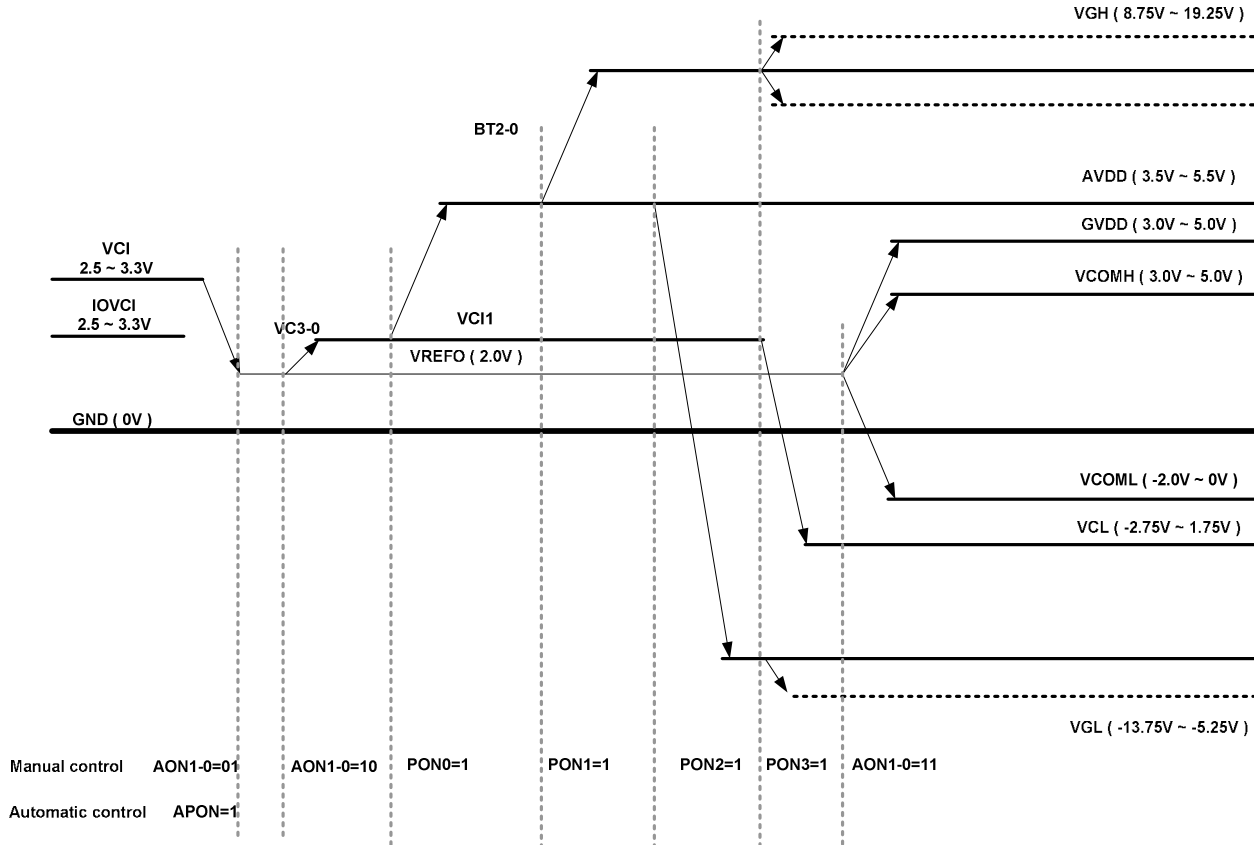


Figure 9-2 : Internal Power Generation Sequence

[NOTE-1] Manual control : AON[1:0], PON0, PON1, PON2, PON3, AON instructions are separately offered for flexibility of power-up sequence time control.

[NOTE-2] Automatic control : APON instruction is an auto power-up sequence operation register. This operation takes more than 9 frame times at RGB interface mode and 105ms at Internal Display mode.

Configuration for the internal power generation (AVDD, VGL/VGH, VCL)

The following is the step-up capacitor connection. Many step-up variations can be chosen with the combination of BT register setting and this connection.

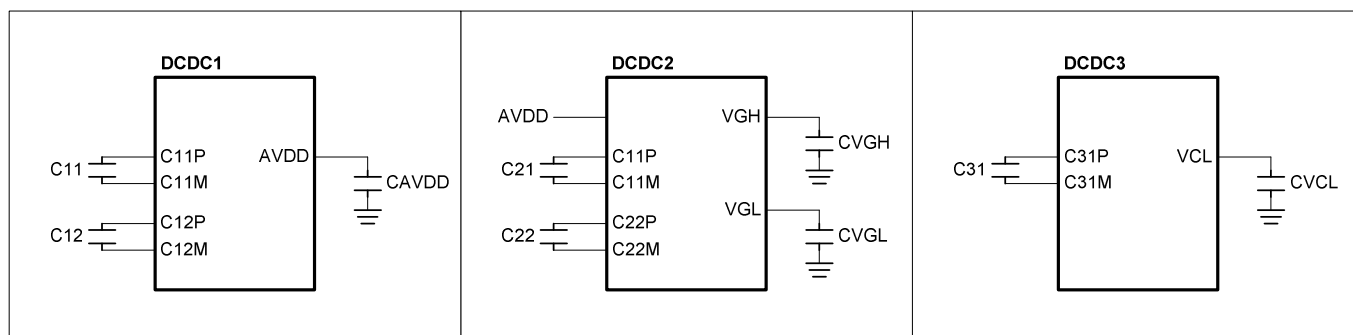


Figure 9-3 : Configuration for AVDD, VGL/VGH, VCL generation

9.4. External Elements for Internal Power Generation

The following tables show specifications of external elements connected to the D51E5TA7601's power supply circuit.

Table 9-2 : Recommended Capacitors

Capacitor connection A capacitor is connected between (A) and (B).		Purpose	Capacitance (μ F)	Rated voltage (V)
(A)	(B)			
C11P	C11M	Flying capacitor	1	10
C12P	C12M		1	10
C21P	C21M		1	16
C22P	C22M		1	25
C31P	C31M		1	10
VCI1	GND	Smoothing capacitor	1	10
RVDD	GND		1	6
VREFO	GND		1	6
AVDD	GND		1	10
VGH	GND		1	25
VGL	GND		1	25
VCL	GND		1	10
GVDD	GND		1	10
VCOMH	GND		1	10
VCOML	GND		1	10

[NOTE] Please make sure that all the capacitors are of grade B concerning temperature, frequency and applied voltage.

Table 9-3 : Recommended Schottky diode

Feature	Pin connection
VF<0.4V / 20mA at 25°C, VR \geq 30V (Recommended diode : HSC226)	VGL – GND

Table 9-4 : Recommended variable resistor

Feature	Pin connection
1~5 $M\Omega$	VCOMR (External variable resistor input pin) Place an external resistor between GVDD and GND

10. Host Interface

The D51E5TA7601 incorporates ten System Interfaces which are used to set instructions, and an RGB Interface that is used to display motion pictures. Selecting one of these interfaces to match the screen data (motion picture or still picture) enables efficient transfer of data for display.

The External Clock Operation mode that uses an RGB Interface allows flicker-free screen update. In this mode, the synchronization signals (VSYNC, HSYNC, and DOTCLK) are available for display operation. The data for display (DB[17:0]) is written according to the status of ENABLE in synchronization with VSYNC, HSYNC, and DOTCLK. In addition, using Window Address Function enables rewriting only to the internal DDRAM area to display motion pictures. Using this function also enables simultaneously display of motion picture and the DDRAM data that was written earlier.

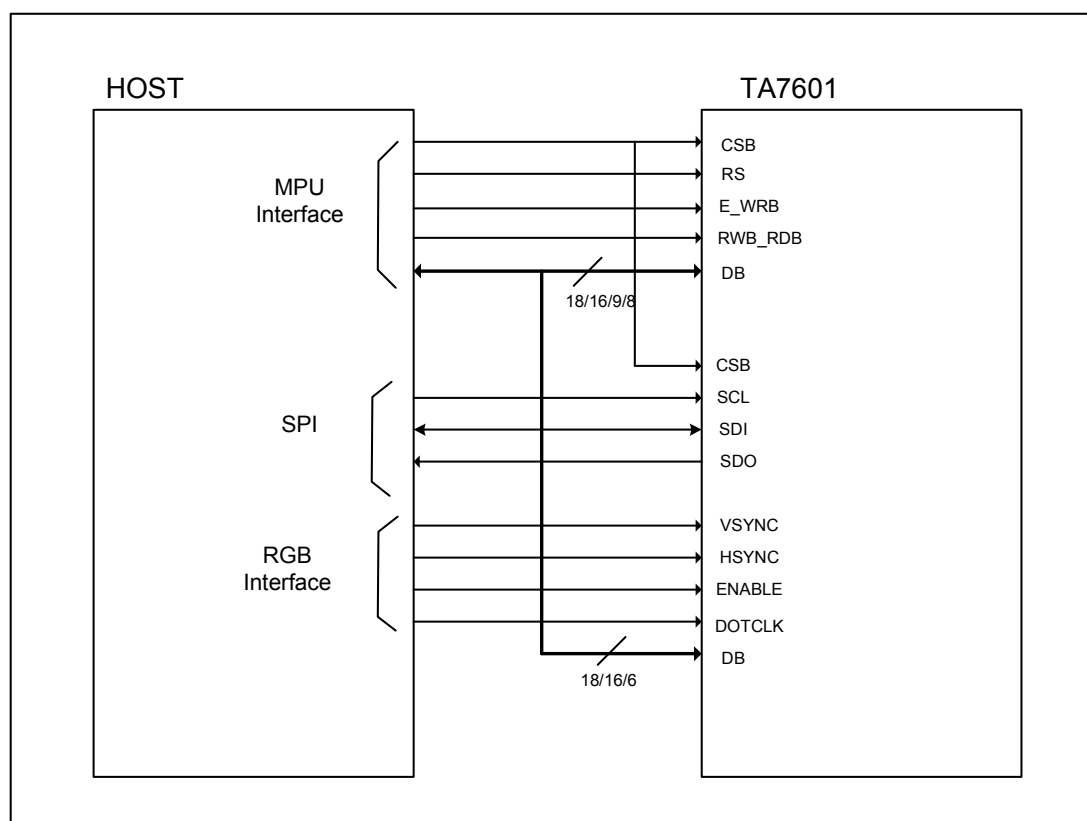


Figure 10-1 : System Interface, RGB Interface

10.1. System Interface

The D51E5TA7601 has twelve system interfaces and 1 high speed serial interface as below.

Table 10-1 : System Interfaces

Interface Type	Pin	Description
	IM[3:0]	
MPU0	4'b0000	M68-system, 16-bit bus interface
MPU1	4'b0001	M68-system, 8-bit bus interface
MPU2	4'b0010	I80-system, 16-bit bus interface
MPU3	4'b0011	I80-system, 8-bit bus interface
MPU4	4'b010x	Serial Peripheral Interface. IM[0] is used as ID pin, 16-bit stream (SPI3="H" : 3-wire, SPI3="L" : 4-wire)
MPU6	4'b011x	Serial Peripheral Interface. IM[0] is used as ID pin, 18-bit stream (SPI3="H" : 3-wire, SPI3="L" : 4-wire)
MPU8	4'b1000	M68-system, 18-bit bus interface
MPU9	4'b1001	M68-system, 9-bit bus interface
MPU10	4'b1010	I80-system, 18-bit bus interface
MPU11	4'b1011	I80-system, 9-bit bus interface
-	4'b1100	Reserved
-	4'b1110	Reserved
-	4'b1101	Reserved
-	4'b1111	Reserved

In order to select one of them, you should set IM[3:0] properly.

M68/18-BIT MPU INTERFACE

Bit Assignment

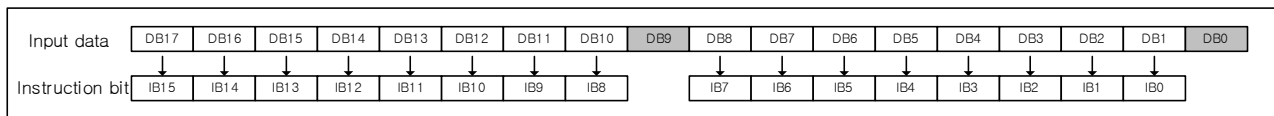


Figure 10-2 : Bit Assignment of instructions on M68/18-bit MPU interface

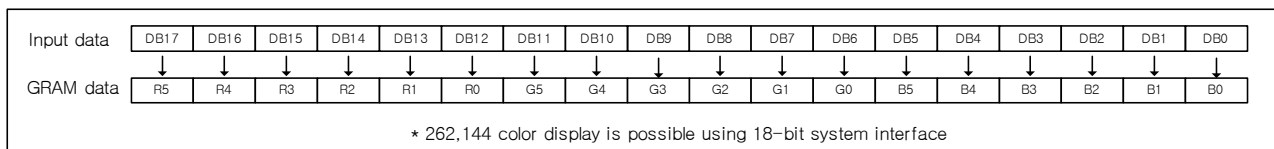
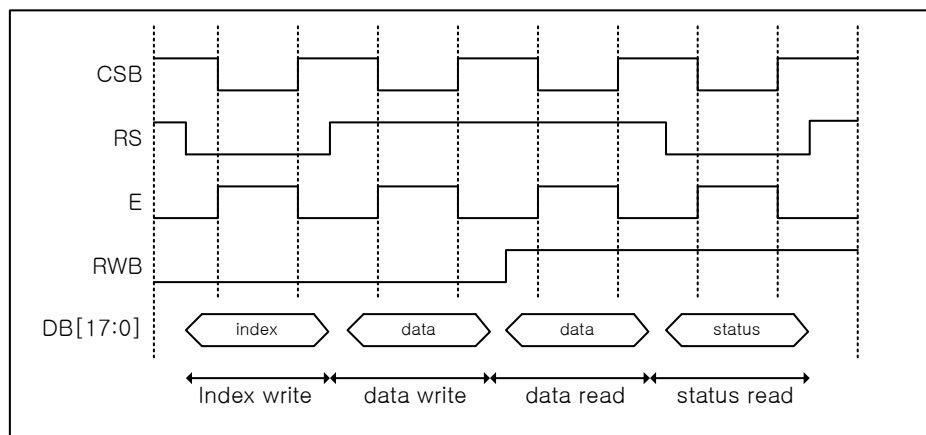


Figure 10-3 : Bit Assignment of DDRAM data on M68/18-bit MPU interface

Timing Diagram

There are 4 timing conditions for M68/18-bit MPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.



[NOTE] There is dummy cycle when memory data is read (see R22h). However, there is no dummy cycle when register data is read.

Figure 10-4 : Timing Diagram of M68/18-bit MPU interface

M68/16-BIT MPU INTERFACE

Bit Assignment

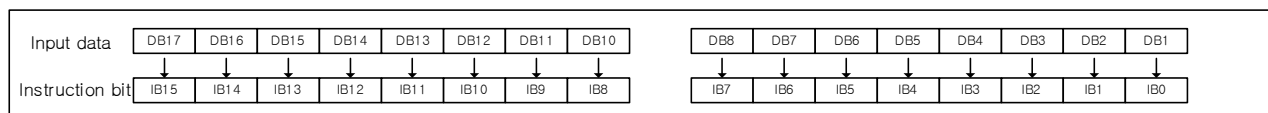


Figure 10-5 : Bit Assignment of instructions on M68/16-bit MPU interface

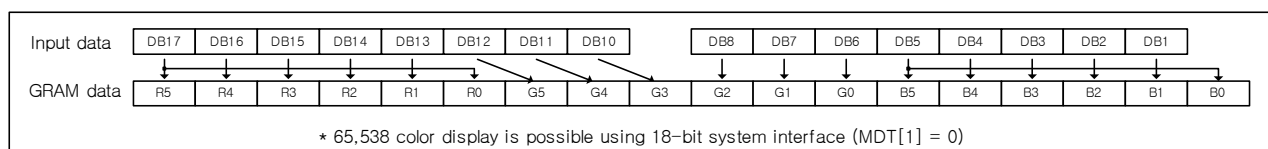
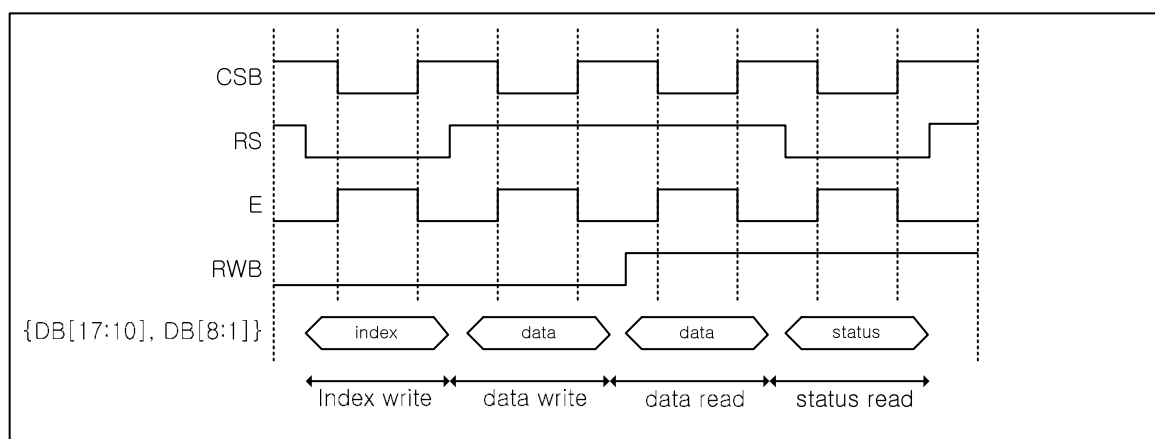


Figure 10-6 : Bit Assignment of DDRAM data on M68/16-bit MPU interface

Timing Diagram

There are 4 timing conditions for M68/16-bit MPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.



[NOTE] There is dummy cycle when memory data is read (see R22h). However, there is no dummy cycle when register data is read.

Figure 10-7 : Timing Diagram of M68/16-bit MPU interface

M68/9-BIT MPU INTERFACE

Bit Assignment

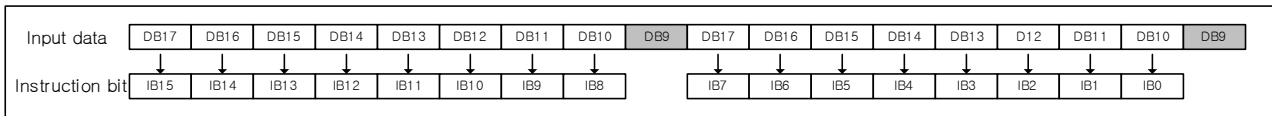


Figure 10-8 : Bit Assignment of instructions on M68/9-bit MPU interface

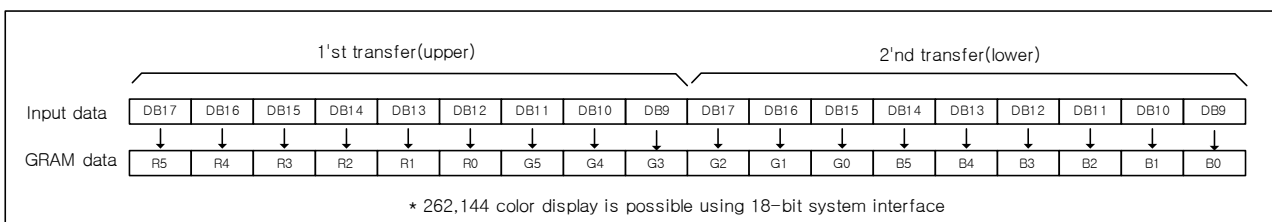
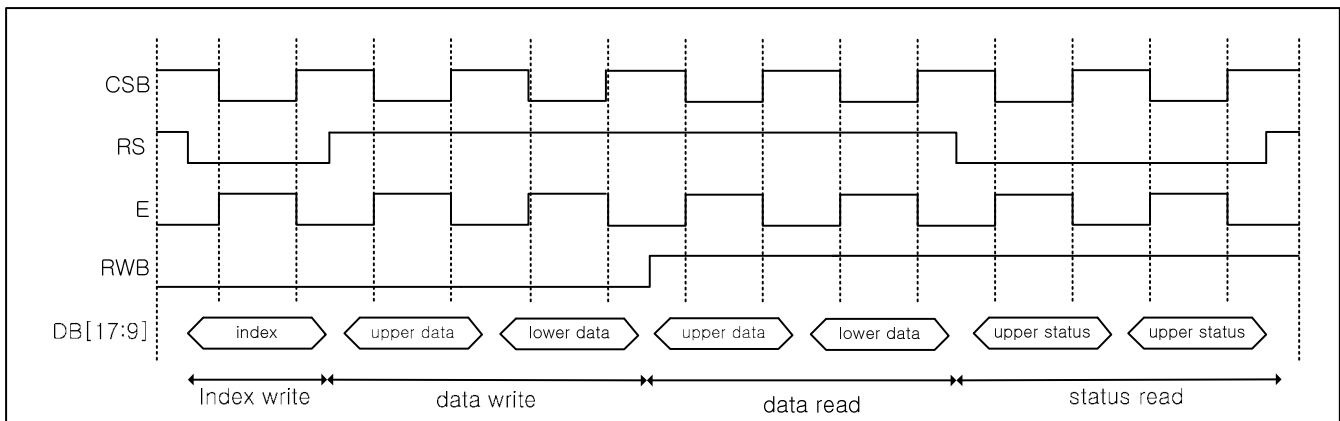


Figure 10-9 : Bit Assignment of DDRAM data on M68/9-bit MPU interface

Timing Diagram

There are 4 timing conditions for M68/9-bit MPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition. In this mode, 16-bit instructions and DDRAM data are divided into two half words and the transfer starts from the upper half word.



[NOTE] There is dummy cycle when memory data is read (see R22h). However, there is no dummy cycle when register data is read. In this case, dummy cycle is 2.

Figure 10-10 : Timing Diagram of M68/9-bit MPU interface

M68/8-BIT MPU INTERFACE

Bit Assignment

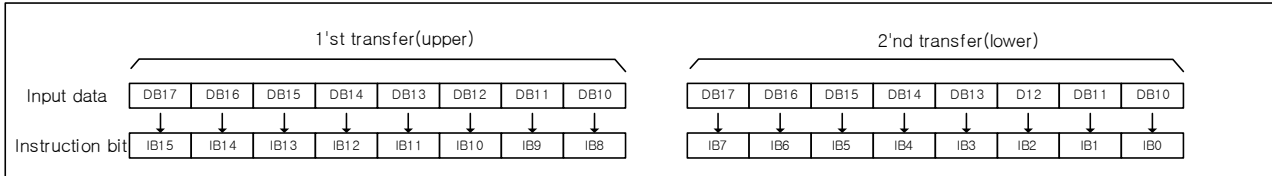


Figure 10-11 : Bit Assignment of instructions on M68/8-bit MPU interface

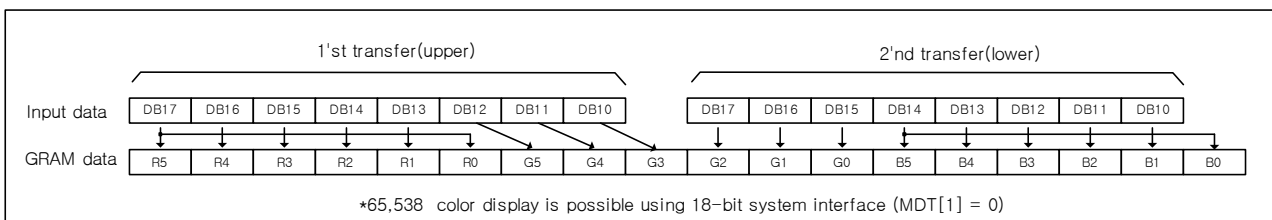
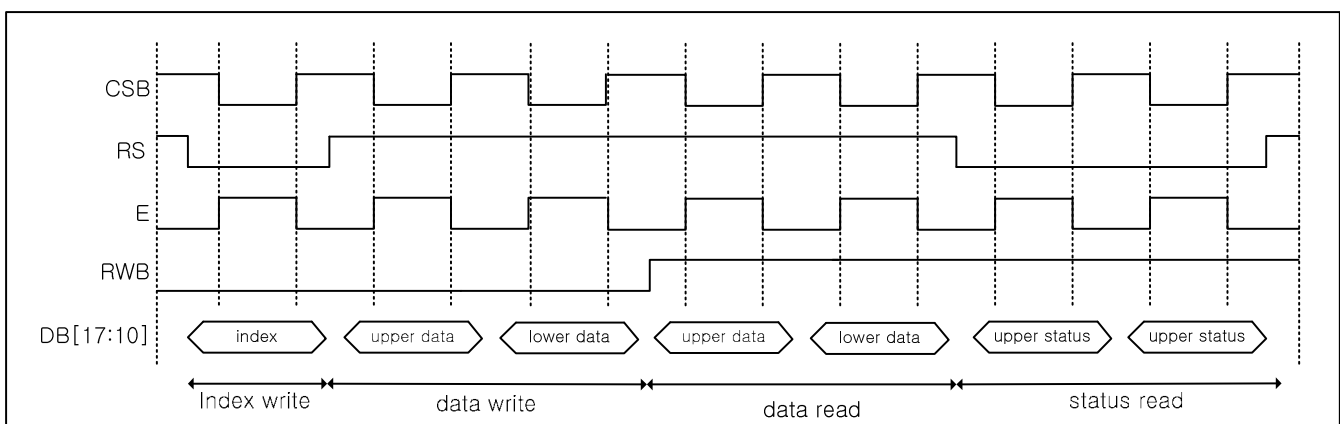


Figure 10-12 : Bit Assignment of DDRAM data on M68/8-bit MPU interface

Timing Diagram

There are 4 timing conditions for M68/8-bit MPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition. In this mode, 16-bit instructions and DDRAM data are divided into two half words and the transfer starts from the upper half word.



[NOTE] There is dummy cycle when memory data is read (see R22h). However, there is no dummy cycle when register data is read. In this case, dummy cycle is 2.

Figure 10-13 : Timing Diagram of M68/8-bit MPU interface

I80/18-BIT MPU INTERFACE

Bit Assignment

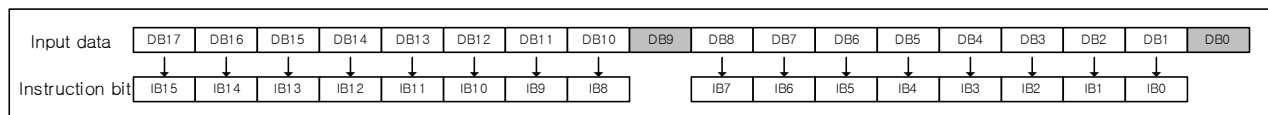


Figure 10-14 : Bit Assignment of instructions on I80/18-bit MPU interface

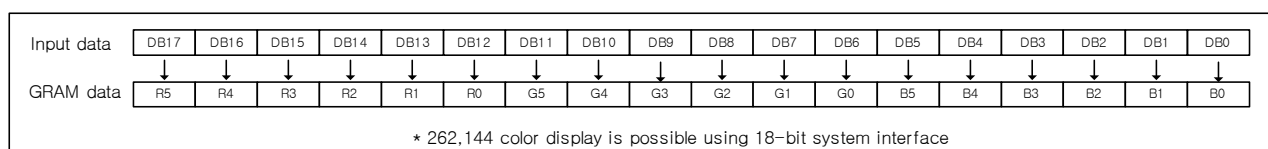
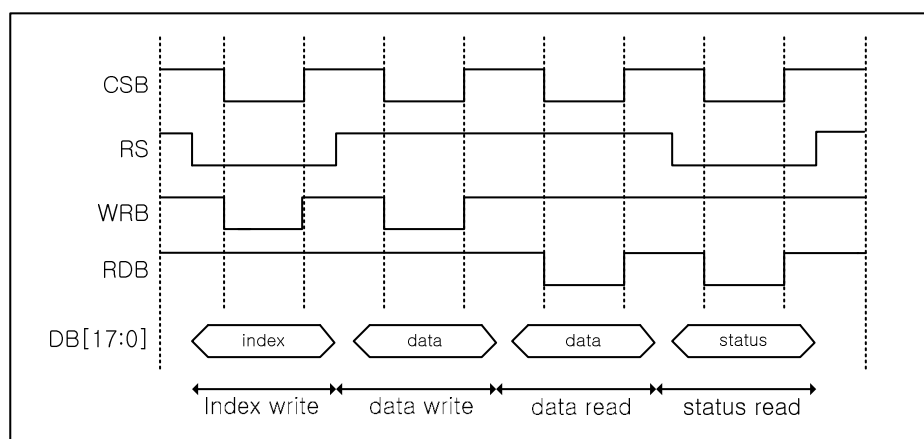


Figure 10-15 : Bit Assignment of DDRAM data on I80/18-bit MPU interface

Timing Diagram

There are 4 timing conditions for I80/18-bit MPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.



[NOTE] There is dummy cycle when memory data is read (see R22h). However, there is no dummy cycle when register data is read.

Figure 10-16 : Timing Diagram of I80/18-bit MPU interface

I80/16-BIT MPU INTERFACE

Bit Assignment

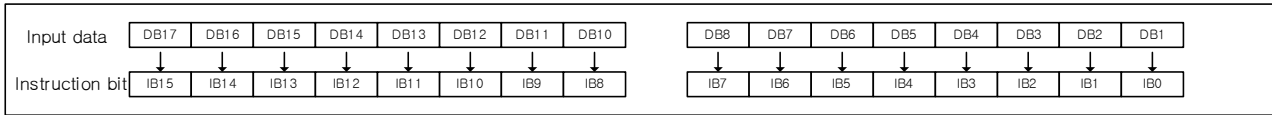


Figure 10-17 : Bit Assignment of instructions on I80/16-bit MPU interface

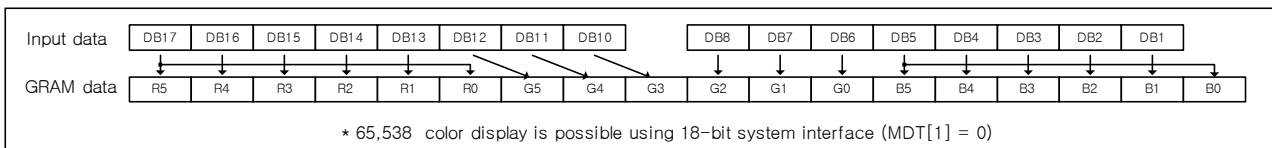
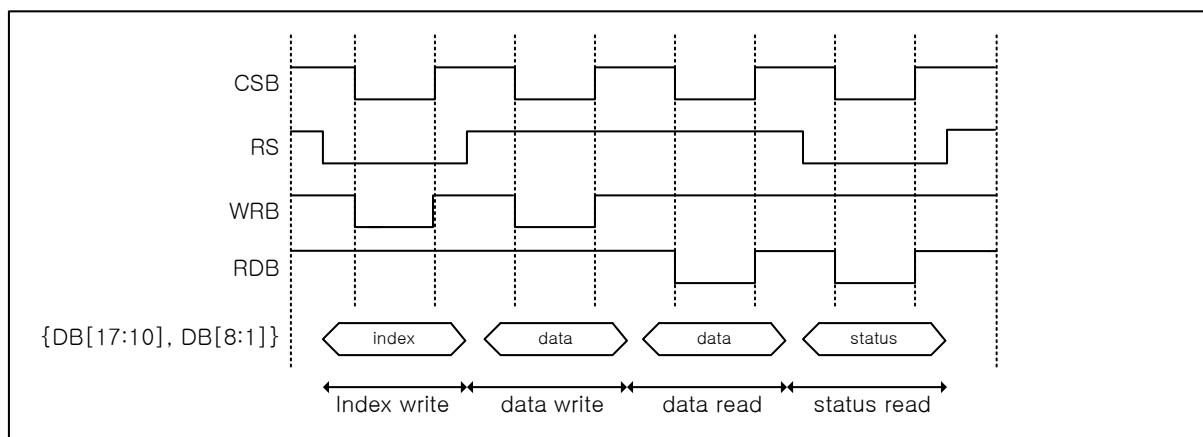


Figure 10-18 : Bit Assignment of DDRAM data on I80/16-bit MPU interface

Timing Diagram

There are 4 timing conditions for I80/16-bit MPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition.



[NOTE] There is dummy cycle when memory data is read (see R22h). However, there is no dummy cycle when register data is read. In this case, dummy cycle is 2.

Figure 10-19 : Timing Diagram of I80/16-bit MPU interface

I80/9-BIT MPU INTERFACE

Bit Assignment

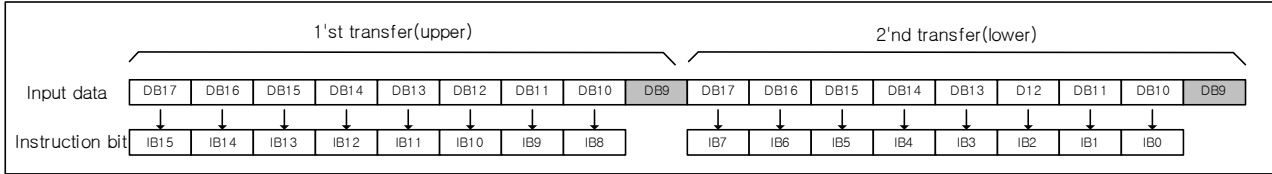


Figure 10-20 : Bit Assignment of instructions on I80/9-bit MPU interface

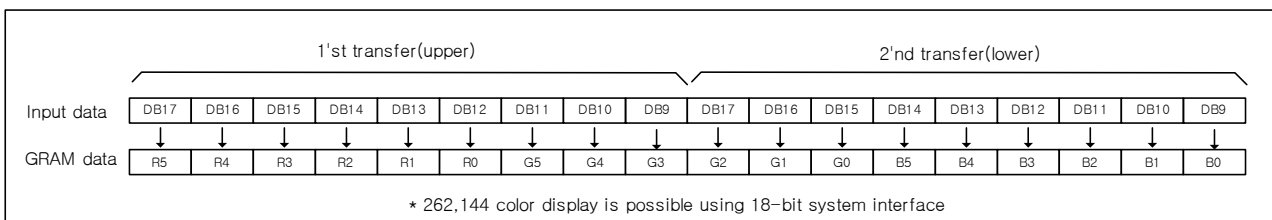
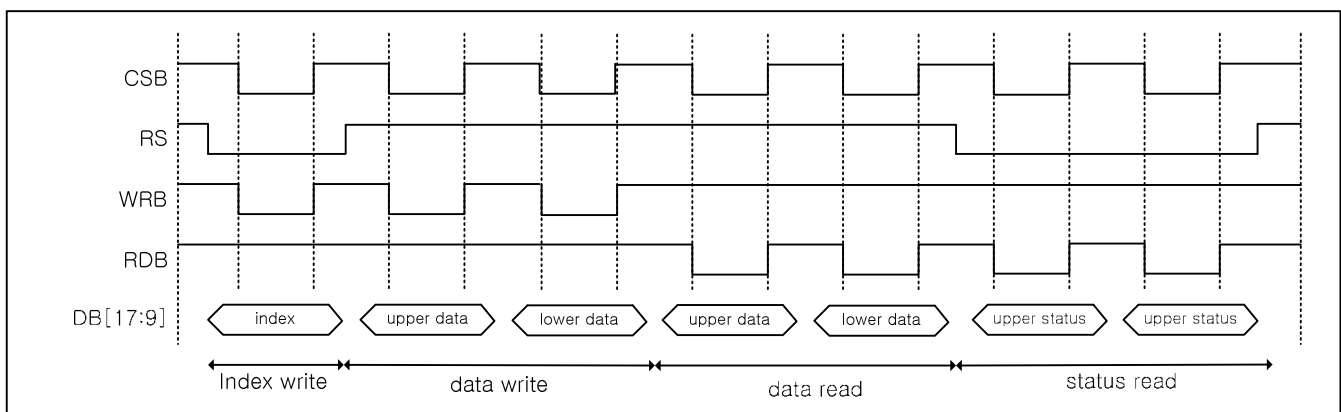


Figure 10-21 : Bit Assignment of DDRAM data on I80/9-bit MPU interface

Timing Diagram

There are 4 timing conditions for I80/9-bit MPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition. In this mode, 16-bit instructions and DDRAM data are divided into two half words and the transfer starts from the upper half word.



[NOTE] There is dummy cycle when memory data is read (see R22h). However, there is no dummy cycle when register data is read. In this case, dummy cycle is 2.

Figure 10-22 : Timing Diagram of I80/9-bit MPU interface

I80/8-BIT MPU INTERFACE

Bit Assignment

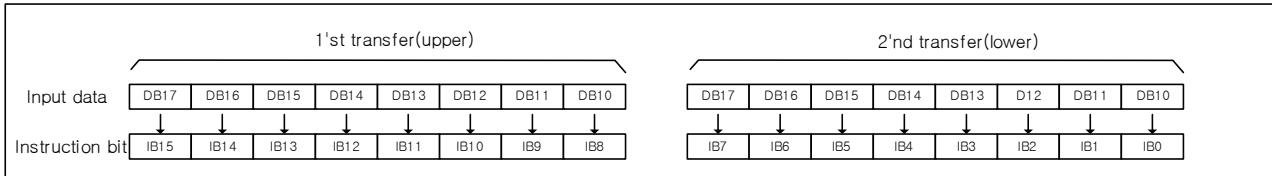


Figure 10-23 : Bit Assignment of instructions on I80/8-bit MPU interface

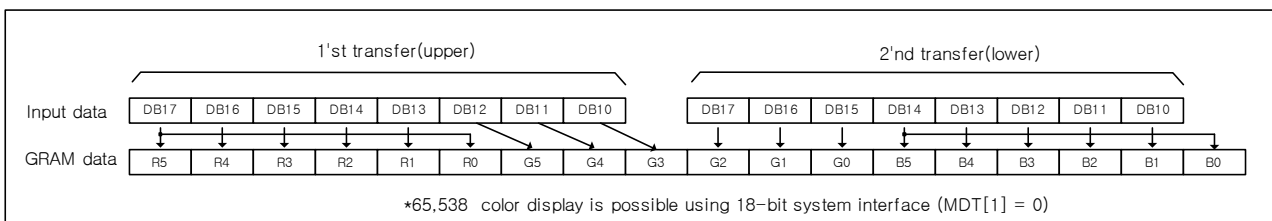
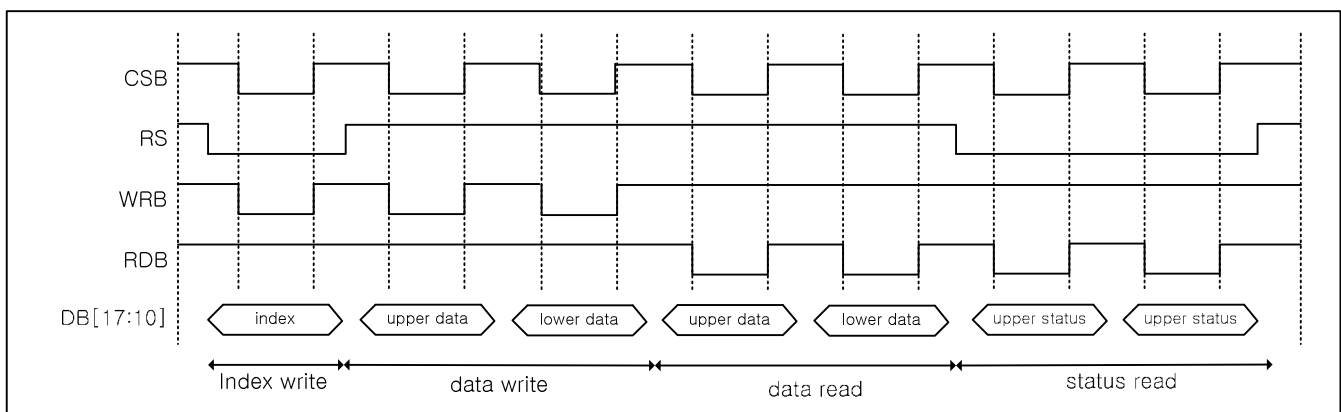


Figure 10-24 : Bit Assignment of DDRAM data on I80/8-bit MPU interface

Timing Diagram

There are 4 timing conditions for I80/8-bit MPU interface, which are index write timing condition, data write timing condition, data read timing condition and status read timing condition. In this mode, 16-bit instructions and DDRAM data are divided into two half words and the transfer starts from the upper half word.



[NOTE] There is dummy cycle when memory data is read (see R22h). However, there is no dummy cycle when register data is read. In this case, dummy cycle is 2.

Figure 10-25 : Timing Diagram of I80/8-bit MPU interface

10.2. Serial Peripheral Interface

Setting IM[3:0] properly allows standard clock-synchronized serial data transfer (SPI : Serial Peripheral Interface), using CSB (chip select), SCL (serial transfer clock), SDI (serial input data) and SDO (serial output data). For the serial interface, IM[0] is used as ID.

The D51E5TA7601 initiates serial data transfer by transferring the start byte at the falling edge of CSB input. It ends serial data transfer at the rising edge of CSB input.

The D51E5TA7601 is selected when the 6-bit chip address in the start byte transferred by the transmitting device matches the 6-bit device identification code assigned to D51E5TA7601. ID is the least significant bit of the device identification code. The D51E5TA7601, when selected, receives the subsequent data string.

Two different chip addresses must be assigned to a single D51E5TA7601 because the 7th bit of the start byte is used as a register select bit (RS) : That is, when RS = "0", data can be written to the index register or status can be read, and when RS = "1", an instruction can be issued or data can be written to or read from DDRAM. Read or write is determined according to the 8th bit of the start byte (RWB bit). The data is written (received) when the RWB bit is "0", and is read (transmitted) when the RWB bit is "1".

After receiving the start byte, the D51E5TA7601 receives or transmits the subsequent data. The data is transferred with the MSB first. All D51E5TA7601 instructions are 16-bit wide, so two bytes are received with the MSB first (bit15 to bit0), and then the instruction is internally executed.

The D51E5TA7601 supports 3-wire/4-wire mode SPI. When SPI3 input is low, the D51E5TA7601 operates 4-wire mode. That is, CSB/SCL/SDI/ SDO signals are required for correct operation.

When SPI3 input is high, the D51E5TA7601 operates 3-wire mode. That is, CSB/SCL/SDI signals are required for correct operation. In this case, SDI is bidirectional I/O. For details, see the timing diagram shown below.

The D51E5TA7601 supports both 18-bit stream and 16-bit stream. When IM[3:0] is 4'b010x, 16-bit stream is transferred through SPI. When IM[3:0] is 4'b011x, 18-bit stream is transferred through SPI. For details, see figures shown below.

One byte of DDRAM data read just after the start byte is invalid. The D51E5TA7601 starts to read correct DDRAM data from the 2nd byte. However, it starts to read correct register/status from the 1st byte.

Table 10-2 : Start Byte Format

Transfer Bit	1 st	2 nd	3 rd	4 th	5 th	6 th	7 th	8 th
Start byte format	Device Identification code						RS	RWB
	0	1	1	1	0	ID		

[NOTE] The IM[0] pin is used as ID

Table 10-3 : RS and RWB bit Function

RS bit	RWB bit	Function
0	0	Set index register
0	1	Read status
1	0	Writes instruction or DDRAM data
1	1	Reads instruction or DDRAM data

Bit Assignment

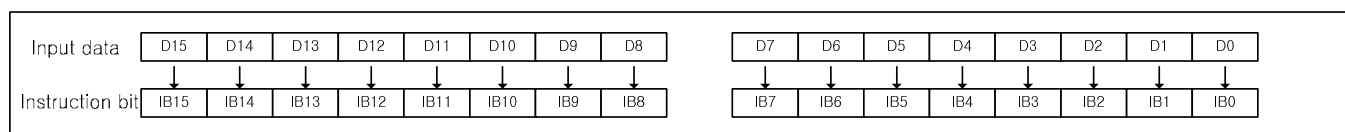


Figure 10-26 : Bit Assignment of instructions on SPI 16-bit mode

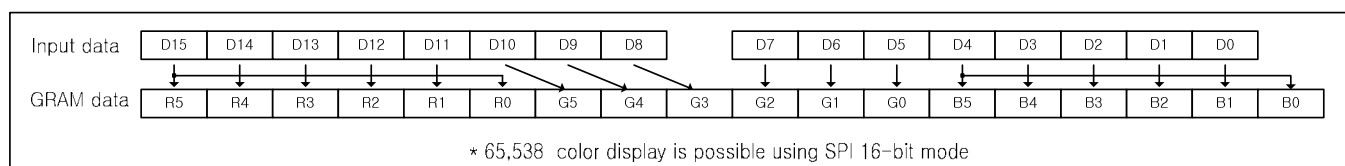


Figure 10-27 : Bit Assignment of DDRAM data on SPI 16-bit mode

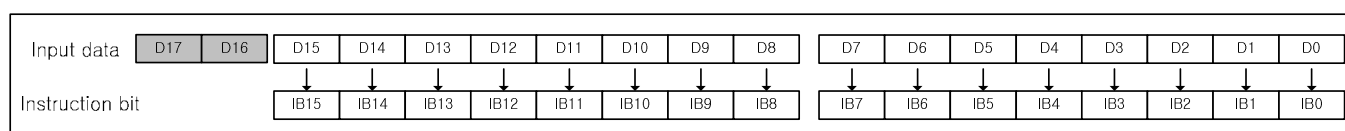


Figure 10-28 : Bit Assignment of instructions on SPI 18-bit mode

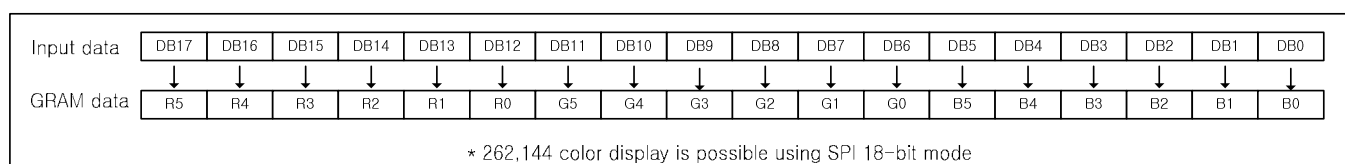


Figure 10-29 : Bit Assignment of DDRAM data on SPI 18-bit mode

Timing Diagrams

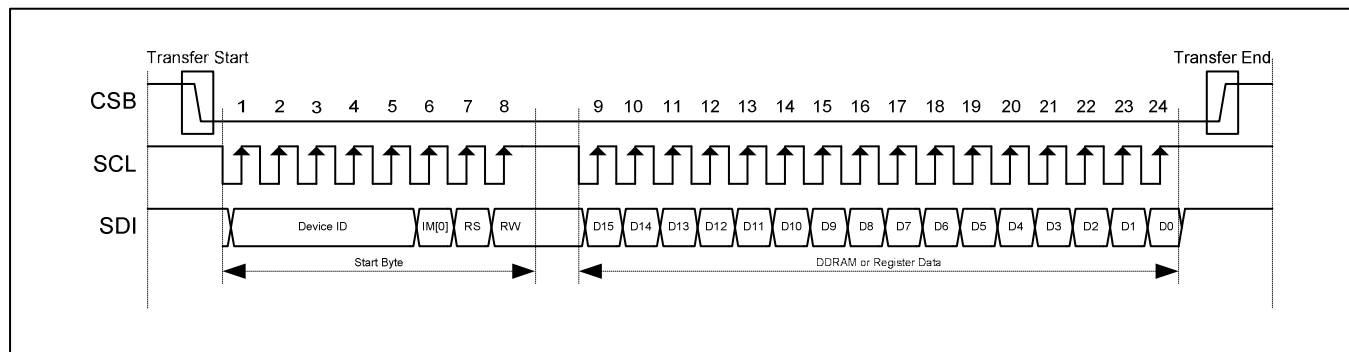


Figure 10-30 : Basic Timing Diagram of Data Transfer through SPI 16-bit mode

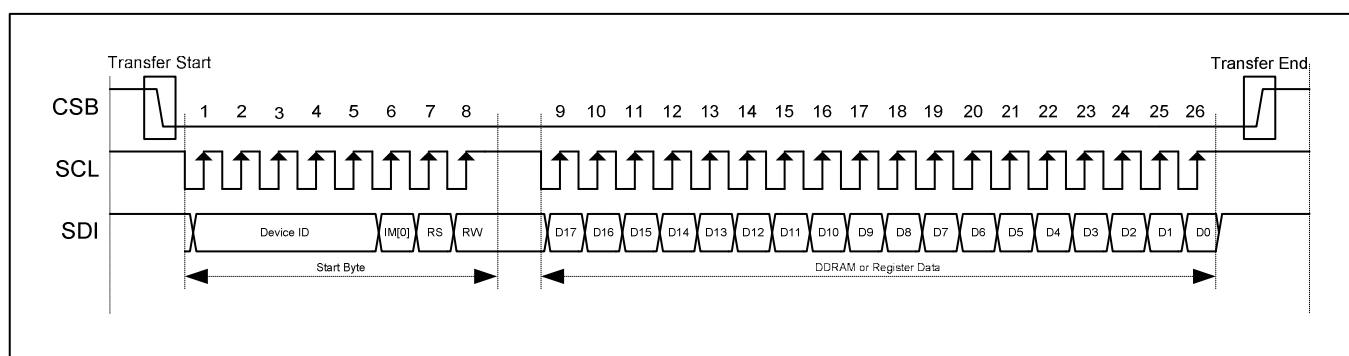


Figure 10-31 : Basic Timing Diagram of Data Transfer through SPI 18-bit mode

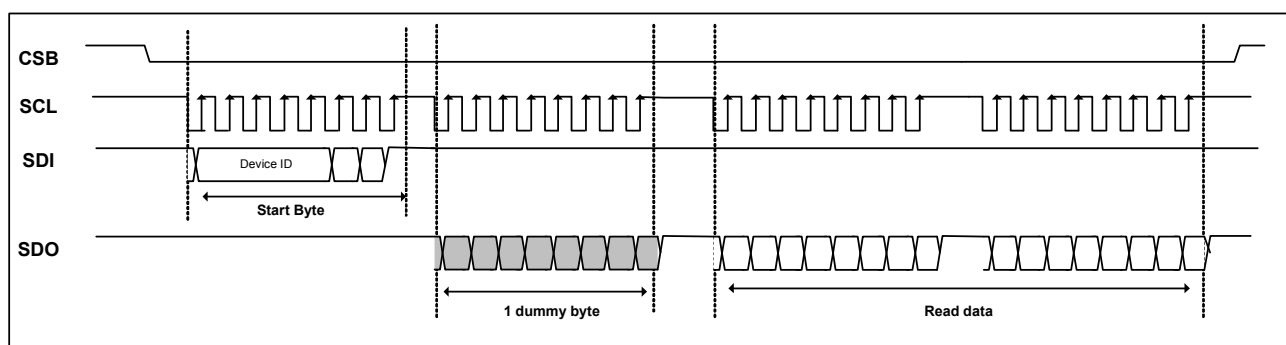


Figure 10-32 : 4-wire mode Timing Diagram of DDRAM-data Read through SPI

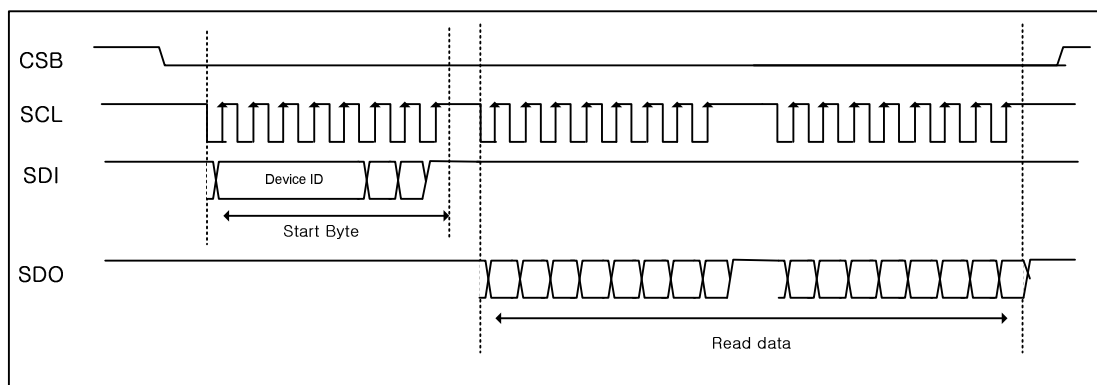


Figure 10-33 : 4-wire mode Timing Diagram of Register/Status-data Read through SPI

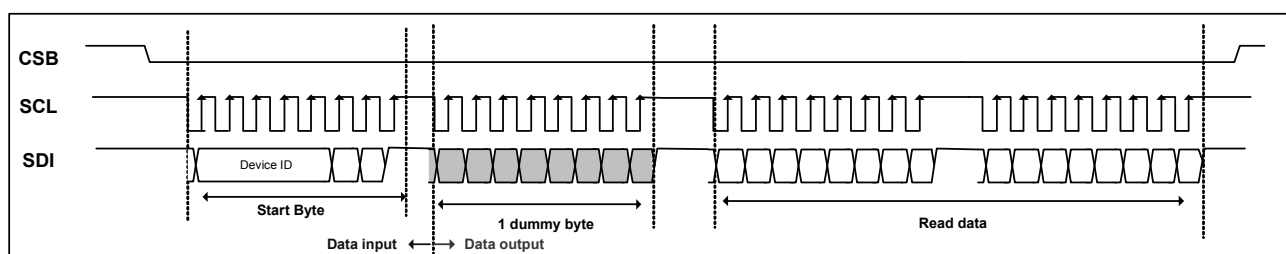


Figure 10-34 : 3-wire mode Timing Diagram of DDRAM-data Read through SPI

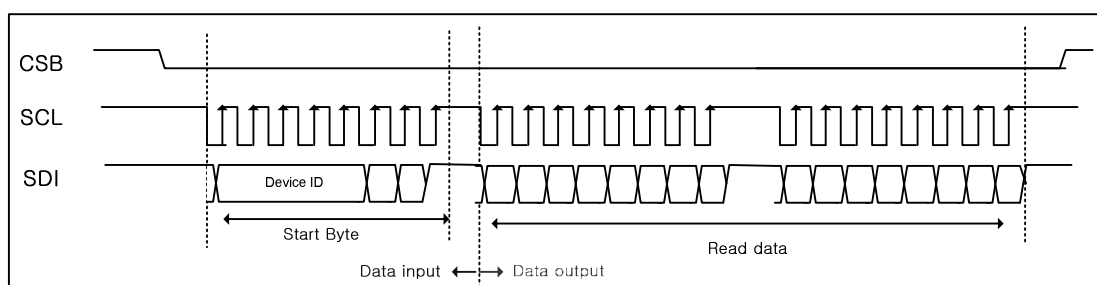


Figure 10-35 : 3-wire mode Timing Diagram of Register/Status-data Read through SPI

10.3. VSYNC Interface

The D51E5TA7601 supports VSYNC interface mode in which D51E5TA7601 executes display operation using internal clock. The internal clock is generated at the internal oscillator and synchronized with the frame synchronization signal, VSYNC. The other signals (HSYNC, Enable and DOTCLK) are not valid in this mode.

When the VSYNC interface mode is selected, the interface displays a moving picture through the system interface with minimum modification that re-writes display data to the DDRAM. The VSYNC interface can be used by setting DM[1:0]=10 and RM=0.

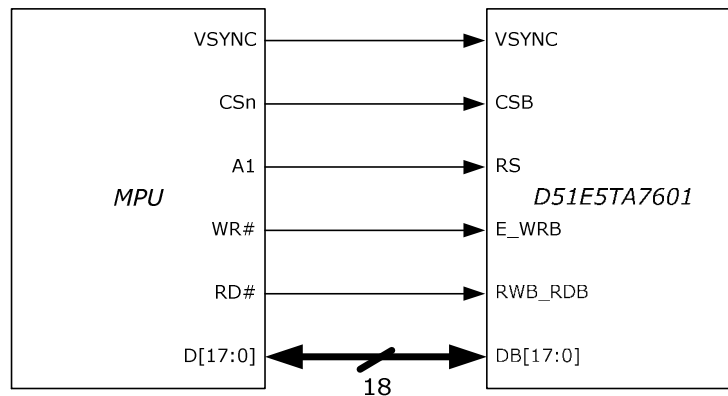


Figure 10-36 : VSYNC Interface to MPU

The VSYNC interface has some constraints between the internal clock and the DDRAM write speed via the system interface. It requires the DDRAM write speed to be faster than the speed at which DDRAM data is displayed. The internal clock of the VSYNC interface can be calculated by the following formula that uses some parameters with FP, BP and display lines[480] :

$$\text{Internal oscillator clock (fosc) [Hz]} = \text{Frame Frequency} \times [480 + \text{FP} + \text{BP}] \times \text{RTN} \times \text{Frequency Fluctuation}$$

The parameter of frequency fluctuation is ascribed to voltage variation, fabrication process condition, external temperature, humidity condition, etc.

When RAM write operation starts at the falling (VSPL="0") edge, the minimum write speed can be calculated by the following formula:

$$\text{The Min. RAM Write Speed [Hz]} \geq \frac{320 \times 480}{\text{Back Porch (BP)} + 480 - \text{Margin Lines}} \times \text{RTN} \times (1/\text{fosc})$$

The margin line(tML in the figure below) means that when operating in VSYNC interface mode, it must be remained the several lines in advance for protection between the actual line of the display operation and the line address for the DDRAM write data operation. The calculated value is the theoretical value that the D51E5TA7601 starts the DDRAM write operation. In other words, the actual value of DDRAM write speed must be larger than the theoretical value that is calculated from the above formula by getting an internal oscillator clock first.

An example of internal oscillator clock and the minimum speed for DDRAM writing set up in VSYNC interface mode is as follows.

Example:

Display size: 320RGB x 480 lines

FP: 2 lines

BP: 14 lines

RTN: 86

Margin Lines (tML) : 2

Frame frequency: 60Hz

$$\text{Internal oscillator clock (fosc)} = 120 \times (480 + 2 + 14) \times 86 = 2.56\text{MHz}$$

$$\text{The minimum RAM write speed} = 320 \times 480 \times 6.26\text{M} / \{[14 + 480 - 2] \times 86\} = 9.29\text{MHz}$$

In this example, the minimum DDRAM write speed of VSYNC interface is 9.29MHz. But, when the starting point of RAM write operation changes the formula described above should be modified accordingly.

When the D51E5TA7601 makes transition from system interface mode to VSYNC interface mode or vice versa, the difference between those modes is the use of VSYNC signal for synchronization. Both system interface mode and VSYNC interface mode use the internal oscillator to generate the reference clock. Figure shown below illustrates the transition flow between the VSYNC interface mode and the system interface mode, which is shown with register settings.

For VSYNC display, the VSYNC should operate as active low pulse and the minimum pulse width is longer than $16/f_{osc}$ when VSPL is set "0."

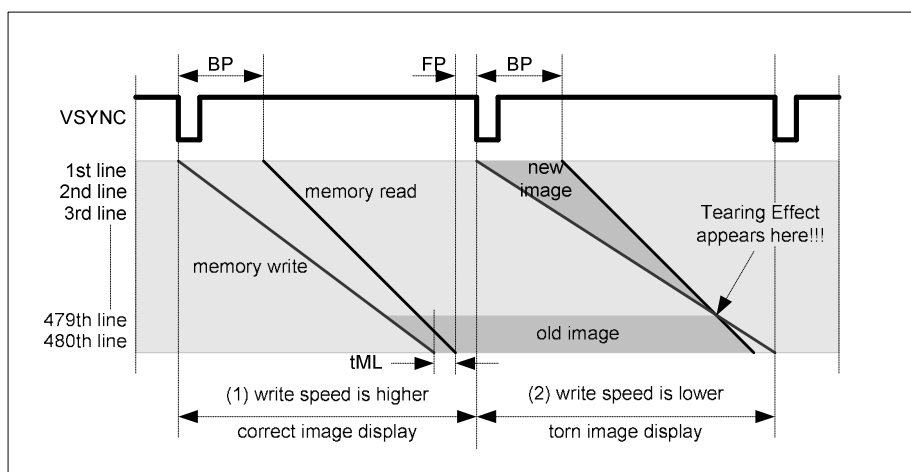


Figure 10-37 : The minimum RAM write speed to avoid Tearing Effect

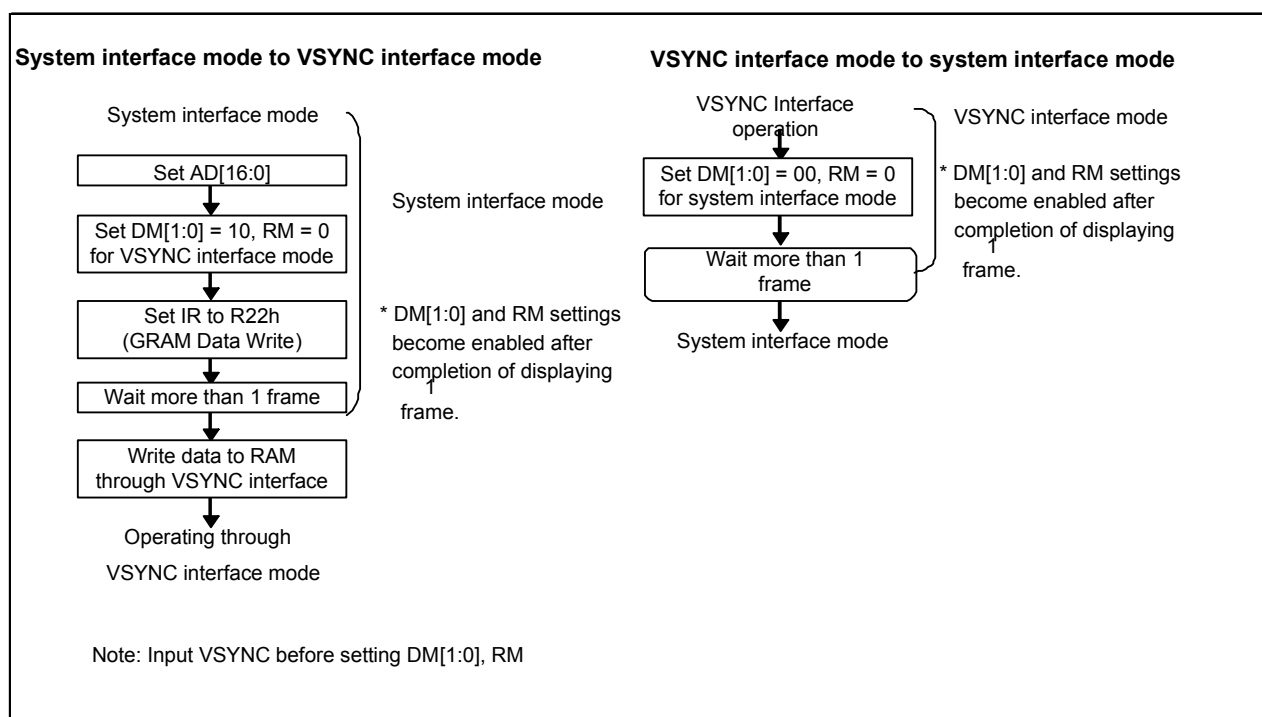


Figure 10-38 : Transition Flow between System Interface Mode and VSYNC Interface Mode

10.4. RGB Interface

The display operation via the RGB interface is synchronized with VSYNC (frame synchronizing signal), HSYNC (line synchronizing signal) and DOTCLK (dot clock). Table shown below describes transferring of display data in a pixel unit via the DB[17:0] bits according to the data enable signal (ENABLE). The RGB interface can be used by setting RM=1. The bus width of interface is selected by setting the RIM[2:0] bit.

Table 10-4 : DDRAM Update with ENABLE & EPL

EPL	ENABLE	DDRAM write	DDRAM Address
0	0	Enable	Update
0	1	Disable	Keep
1	0	Disable	Keep
1	1	Enable	Update

When the D51E5TA7601 is set to operate in RGB interface mode, back porch starts on the falling (when VSPL=0) edge of a VSYNC signal. Just after the back porch, display operation of 480 lines (NL=6'b111100) is performed and after that front porch starts. The front porch continues until the next input of VSYNC signal.

We recommend horizontal porch period should be larger than 12 dot-clocks in 1-transfer mode.

The D51E5TA7601 incorporates RGB interface to display motion picture and DDRAM to store data for display.

To display motion pictures, the D51E5TA7601 has the following features.

- Only motion picture area can be transferred by the Window Address Function.
- Only motion picture area to be rewritten can be transferred selectively.
- Reducing the amount of data transferred enables reduce the power consumption of the whole system.
- Still picture area, such as an icon, can be updated while displaying motion pictures combining with the system interface.

Window Address Function enables transfer only the screen to be updated and reduces the power consumption.

18-BIT RGB INTERFACE

Bit Assignment

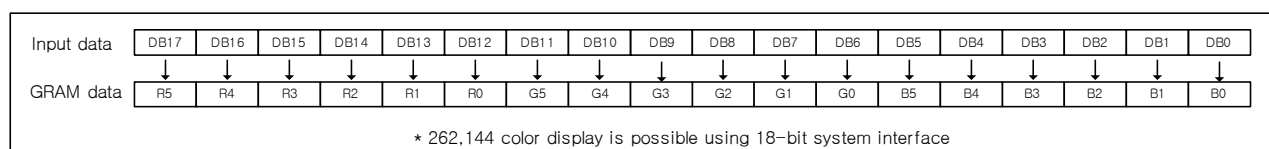


Figure 10-39 : Bit Assignment of DDRAM data on 18-bit RGB Interface

Timing Diagrams

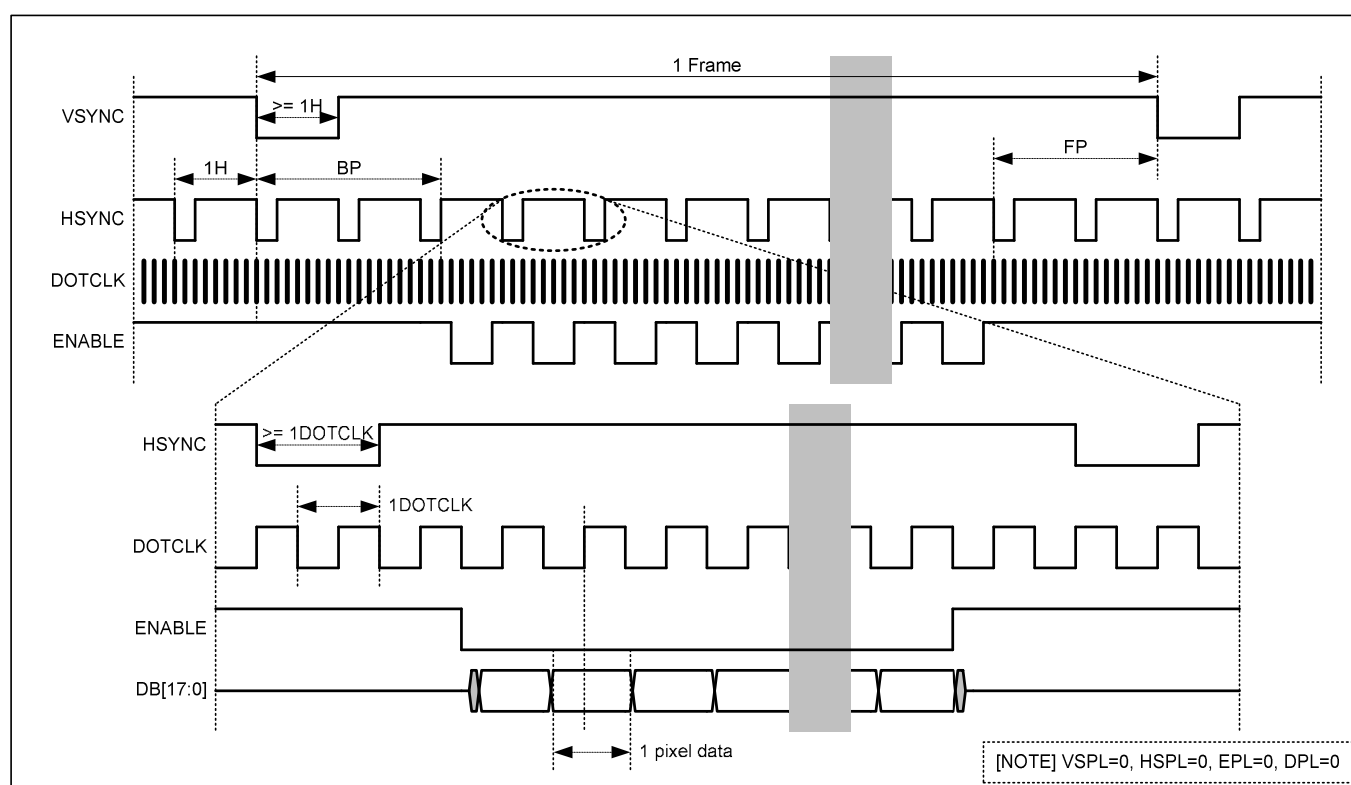


Figure 10-40 : Timing Diagram of 18-bit RGB Interface

16-BIT/1-transfer RGB INTERFACE

Bit Assignment

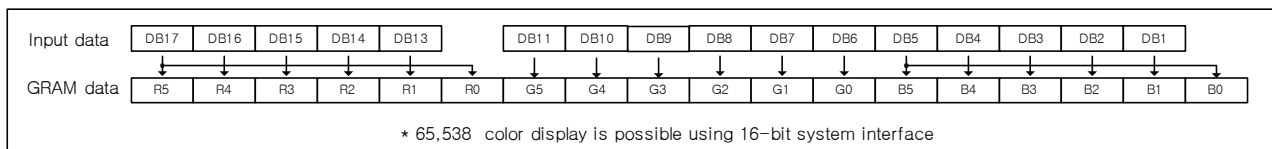


Figure 10-41 : Bit Assignment of DDRAM data on 16-bit/1-transfer RGB Interface

Timing Diagrams

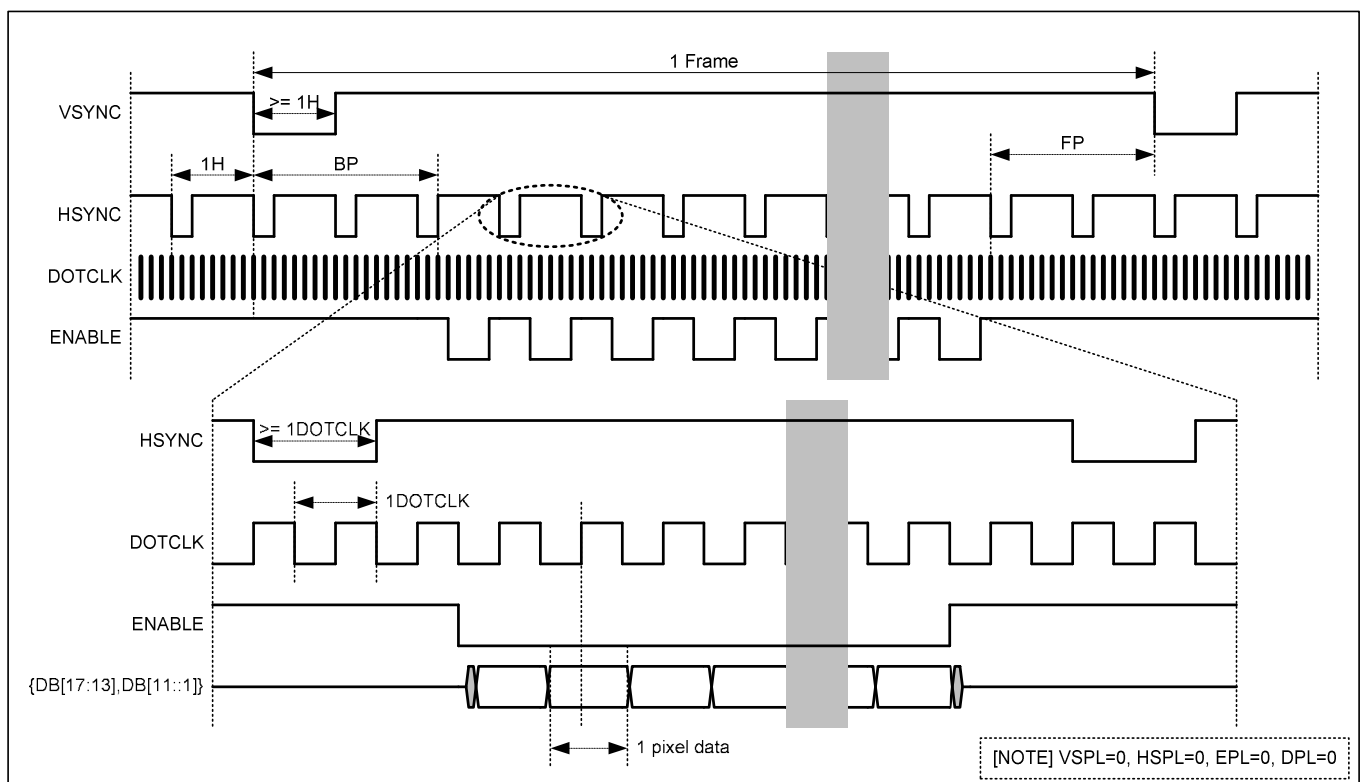


Figure 10-42 : Timing Diagram of 16-bit/1-transfer RGB Interface

16-BIT/2-transfer RGB INTERFACE

Bit Assignment

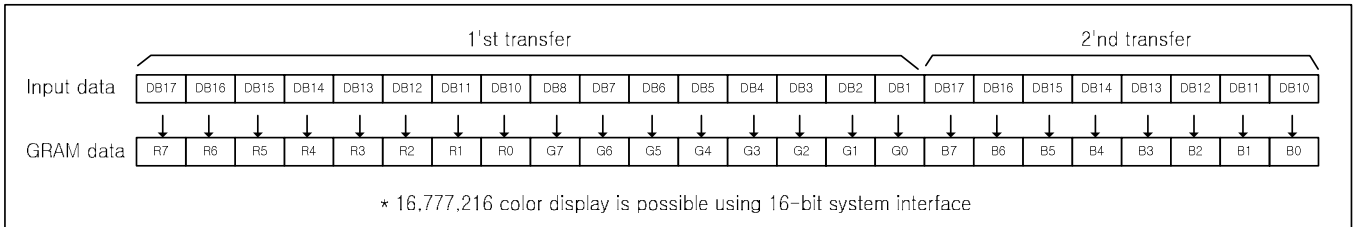


Figure 10-43 : Bit Assignment of DDRAM data on 16-bit/2-transfer RGB Interface

Timing Diagrams

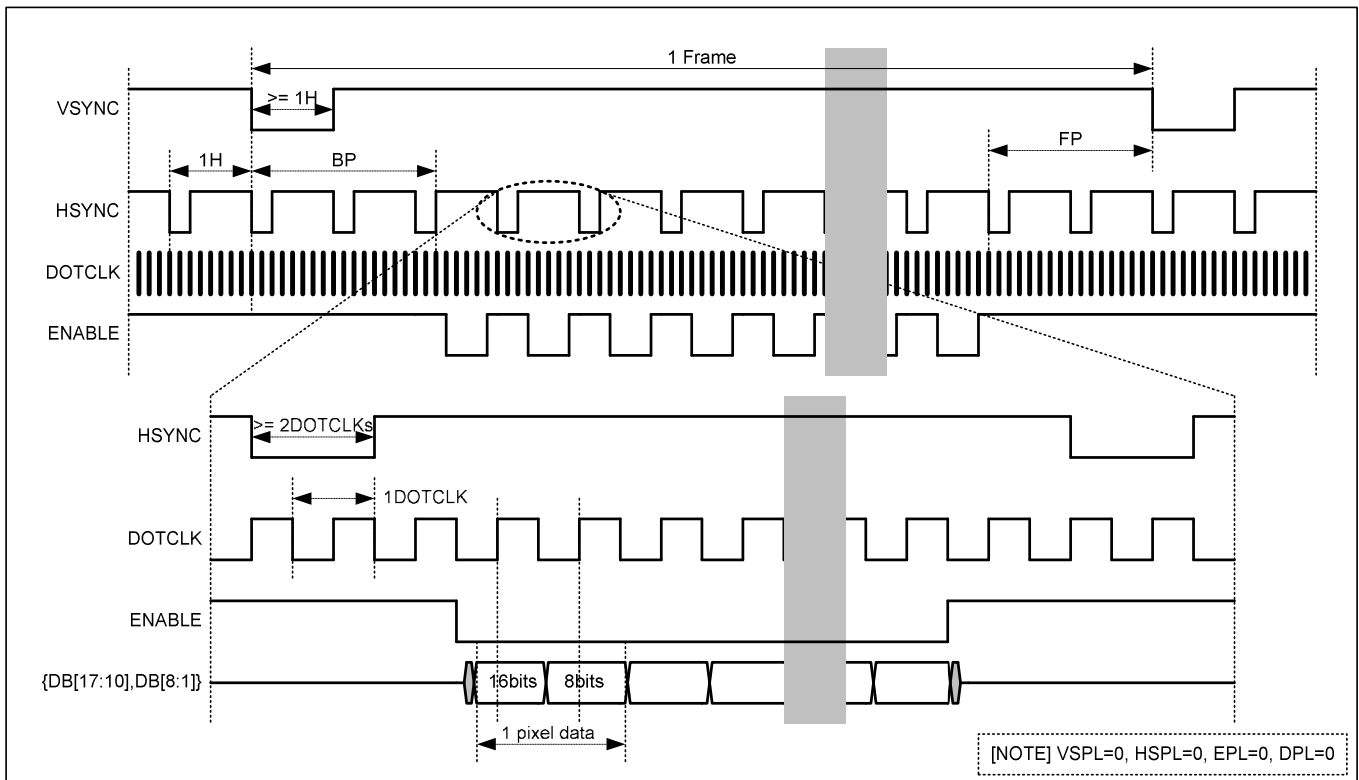


Figure 10-44 : Timing Diagram of 16-bit/2-transfer RGB Interface

In this interface mode,

1. 2 DOTCLK's are regarded as one clock for internal transfer when data is transferred in 16-bit interface.
2. VSYNC, HSYNC, ENABLE, DOTCLK, and DB[17:10] & DB[8:1] should be input in units of two clocks per one pixel.
3. When DOTCLK is not input in units of one pixel, clock mismatch occurs and the frame, which is being operated, and the next frame are not displayed correctly.

8-BIT RGB INTERFACE

Bit Assignment

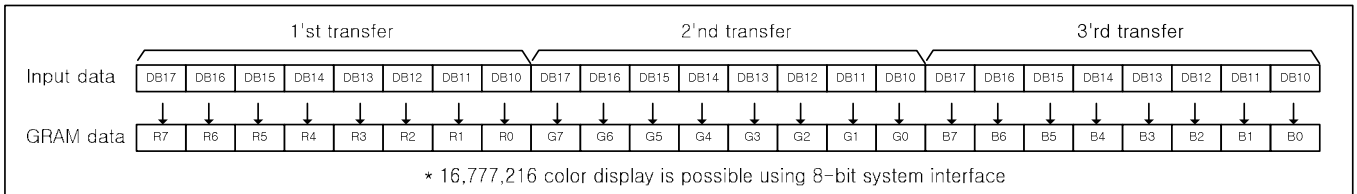


Figure 10-45 : Bit Assignment of DDRAM data on 8-bit RGB Interface

Timing Diagrams

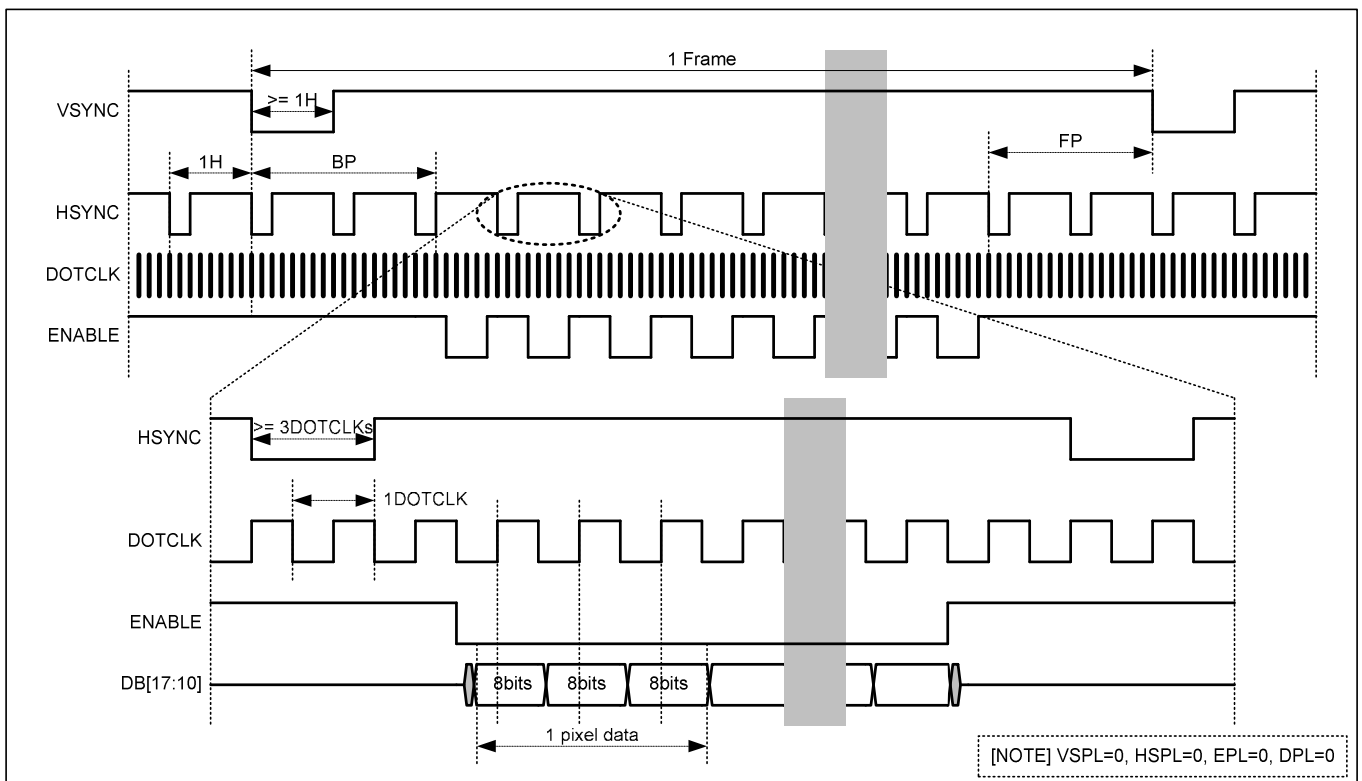


Figure 10-46 : Timing Diagram of 8-bit RGB Interface

In this interface mode,

1. 3 DOTCLK's are regarded as one clock for internal transfer when data is transferred in 8-bit interface.
2. VSYNC, HSYNC, ENABLE, DOTCLK, and DB[17:10] should be input in units of three clocks per one pixel.
3. When DOTCLK is not input in units of one pixel, clock mismatch occurs and the frame, which is being operated, and the next frame are not displayed correctly.

6-BIT RGB INTERFACE

Bit Assignment

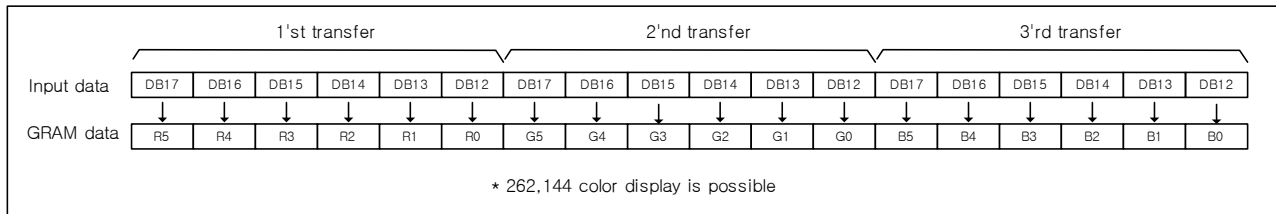


Figure 10-47 : Bit Assignment of DDRAM data on 6-bit RGB Interface

Timing Diagrams

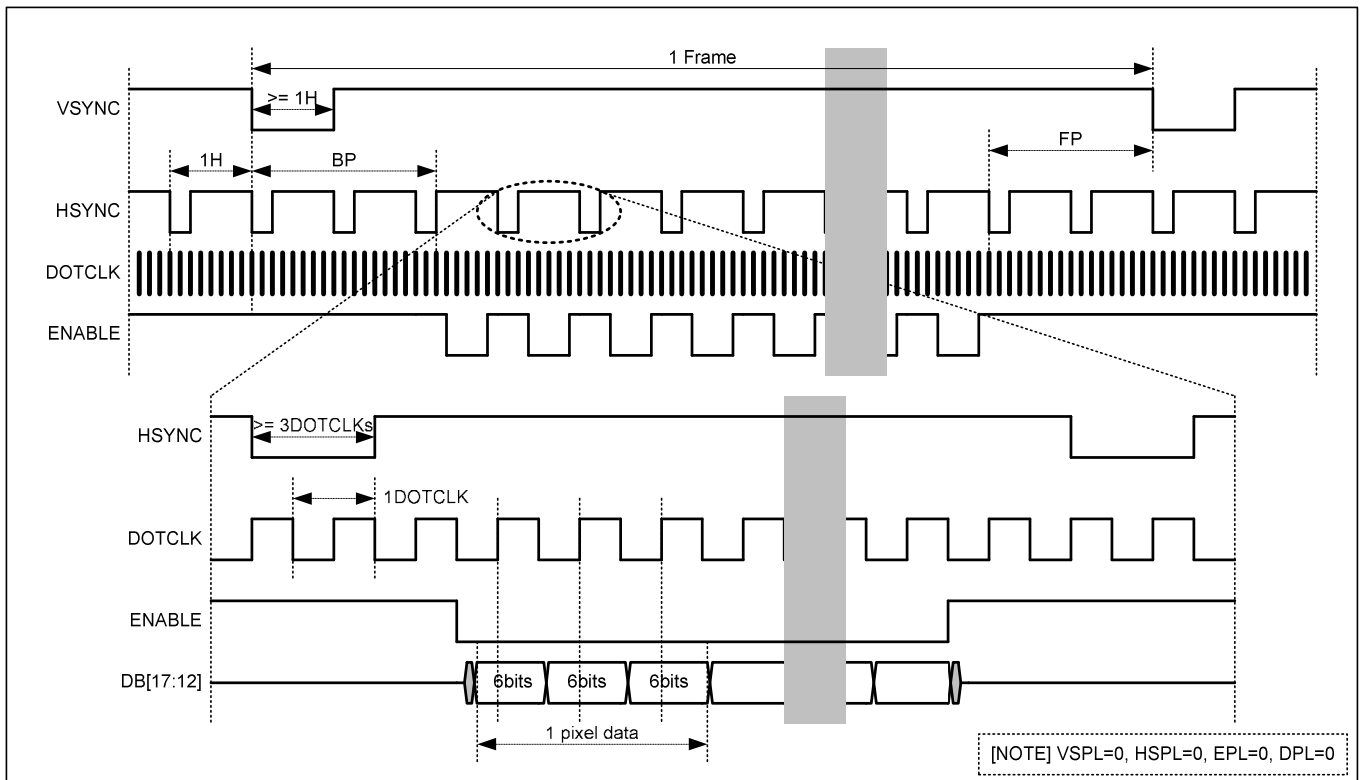


Figure 10-48 : Timing Diagram of 6-bit RGB Interface

In this interface mode,

1. 3 DOTCLK's are regarded as one clock for internal transfer when data is transferred in 6-bit interface.
2. VSYNC, HSYNC, ENABLE, DOTCLK, and DB[17:12] should be input in units of three clocks per one pixel.

When DOTCLK is not input in units of one pixel, clock mismatch occurs and the frame, which is being operated, and the next frame are not displayed correctly.

10.5. Interface Swapping for Memory Access

DISPLAY MODE AND DDRAM ACCESS CONTROL

Display mode and DDRAM access is controlled as shown in blow. For each display status, display mode control and DDRAM access control should be combined properly.

Table 10-5 : DISPLAY MODE & DDRAM ACCESS CONTROL

Display Status	DDRAM Access (RM)	Display Mode (DM[1:0])
1. Still Picture Display	System Interface (RM=0)	Internal Clock Operation (DM[1:0]=00)
2. Motion Picture Display	RGB Interface (RM=1)	External Clock Operation (DM[1:0]=01)
3. Rewrite Still Picture while Motion Picture is being displayed	System Interface (RM=0)	External Clock Operation (DM[1:0]=01)

[NOTE 1] Only system interface can set instruction register.

[NOTE 2] When RGB Interface is being operated, don't change RGB Interface mode (RIM[1:0]).

Internal Clock Operation mode with System Interface (1)

Every operation in internal clock operation mode is done in synchronization with the internal clock which is generated by internal OSC. The signals input through RGB Interface are all meaningless. Access to internal DDRAM is done via system interface.

External Clock Operation mode with RGB Interface (2)

In external clock operation mode, frame sync signal (VSYNC), line sync signal (HSYNC), and DOTCLK are used for display operation. Display data is transferred in the unit of pixel through DB bus and saved to DDRAM.

External Clock Operation mode with System Interface (3)

Write DDRAM data via system interface even in external clock operation mode. There should not be any data transmission on RGB interface in this case. To restart data transmission on RGB interface, set RM to "1", set memory address properly, and write index of 22h for DDRAM write operation.

With the combination of Window Address Function, motion picture and still picture may be saved in separated DDRAM regions respectively. In this case motion picture and still picture are displayed simultaneously.

MOTION PICTURE DISPLAY

This LSI incorporates RGB interface to display motion pictures and DDRAM to store data for display.

For displaying motion pictures, the LSI has following features.

- Only motion picture area can be transferred by the window address function.
- Only motion picture area to be rewritten can be transferred selectively.
- Reducing the amount of data transferred enables reduce the power consumption to the whole system.
- Still picture area, such as icon, can be updated while displaying motion pictures combining with the system interface.

DDRAM ACCESS VIA RGB INTERFACE AND SPI

DDRAM can be accessed via SPI when RGB interface is in use. When data is written to DDRAM during RGB interface mode, ENABLE should be deactivated according to "EPL" bit to stop data writing via RGB interface, because DDRAM writing is always performed in synchronization with DOTCLK input when ENABLE is activated. With "RM" bit set to "0", DDRAM access can be conducted via SPI. After this DDRAM access via SPI, a waiting time is needed for a write bus cycle before the next DDRAM access starts via RGB interface. Of course, in this case, before returning to RGB interface, "RM" bit should be set to "1" and index register should be set up as "R22". When a conflict in DDRAM writing from both RGB interface and SPI occurs, data writing is not guaranteed.

Example of display motion picture via RGB interface and updating still picture via SPI is shown below.

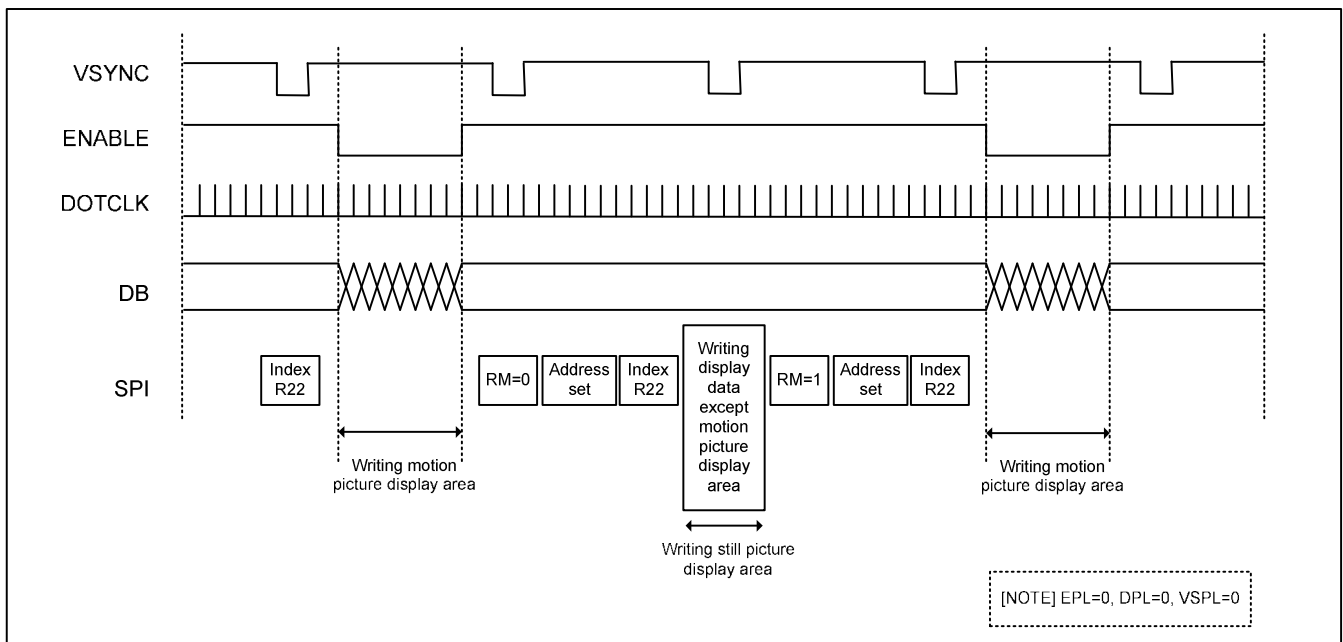


Figure 10-49 : Example of Updating Still Picture Area during Displaying Motion Picture

TRANSITION SEQUENCE BETWEEN DISPLAY MODES

Transition between internal clock operation mode and external clock operation mode should follow the mode transition sequence shown below.

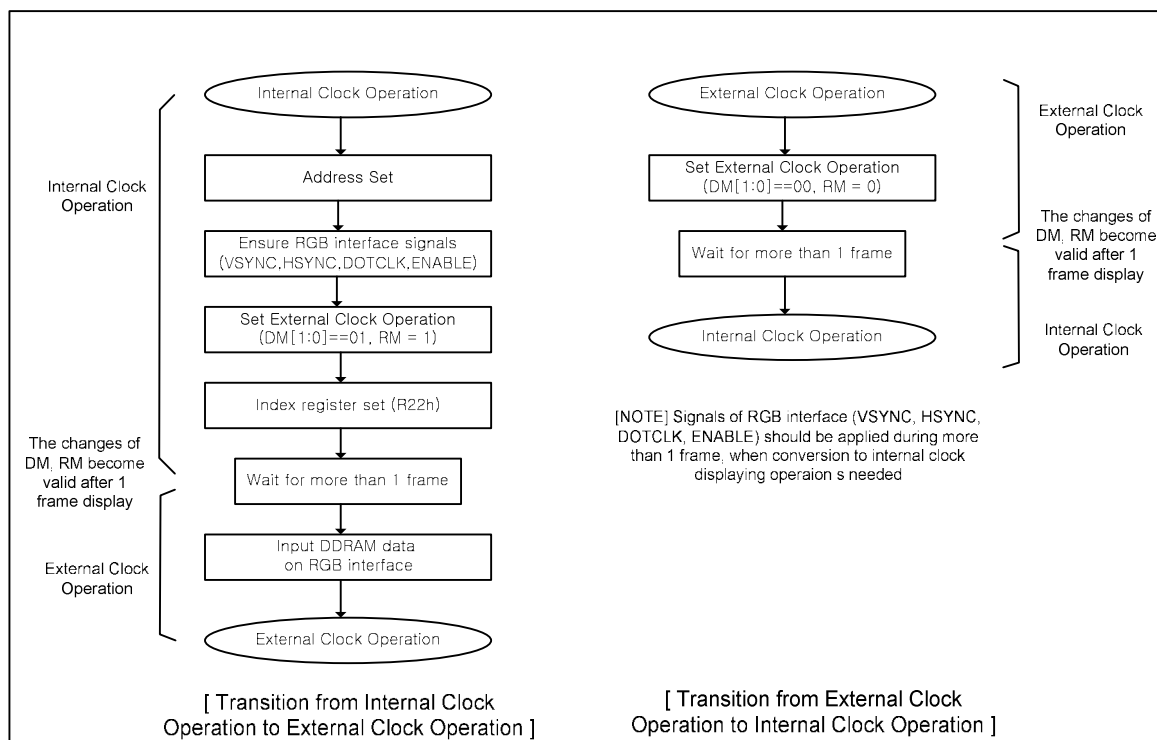


Figure 10-50 : Transition between Internal Clock Operation Mode and External Clock Operation Mode

11. Display Function

11.1. 8-Color Display Mode

The D51E5TA7601 enters 8-color display mode when CL is set as "1." The grayscale level to be used in this mode is only AVDD and VSSA, and the other levels are not used. This, therefore, reduces the power consumption.

In the 8-color mode, the Gamma correction function is invalid. However, the configuration of the Gamma correction registers is retained.

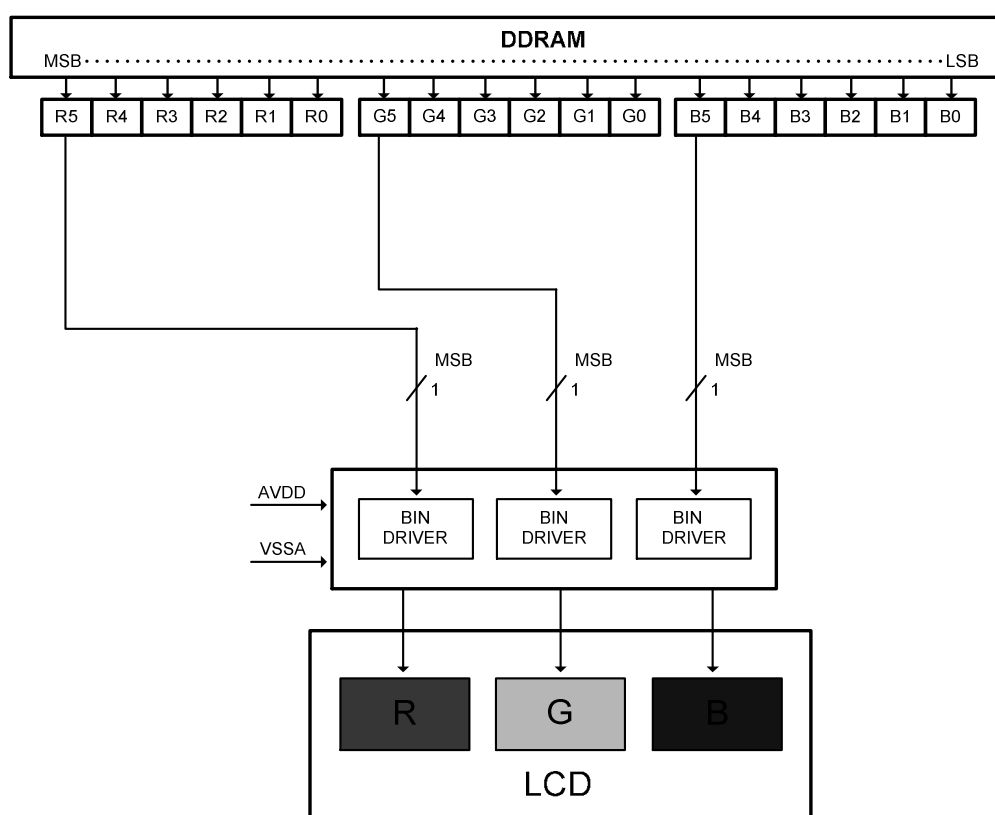


Figure 11-1 : 8-color display mode

11.2. Partial Display Mode

The D51E5TA7601 enters a partial display mode when SPT of the control register is set as “1”. By setting up the partial display control registers (SS1, SE1, SS2, SE2), the D51E5TA7601 can drive one or two screens of any horizontal size at any horizontal position, and specify the colors (black or white) of the non-display areas.

We recommend SMLC_ON register should be “0” in partial display mode.

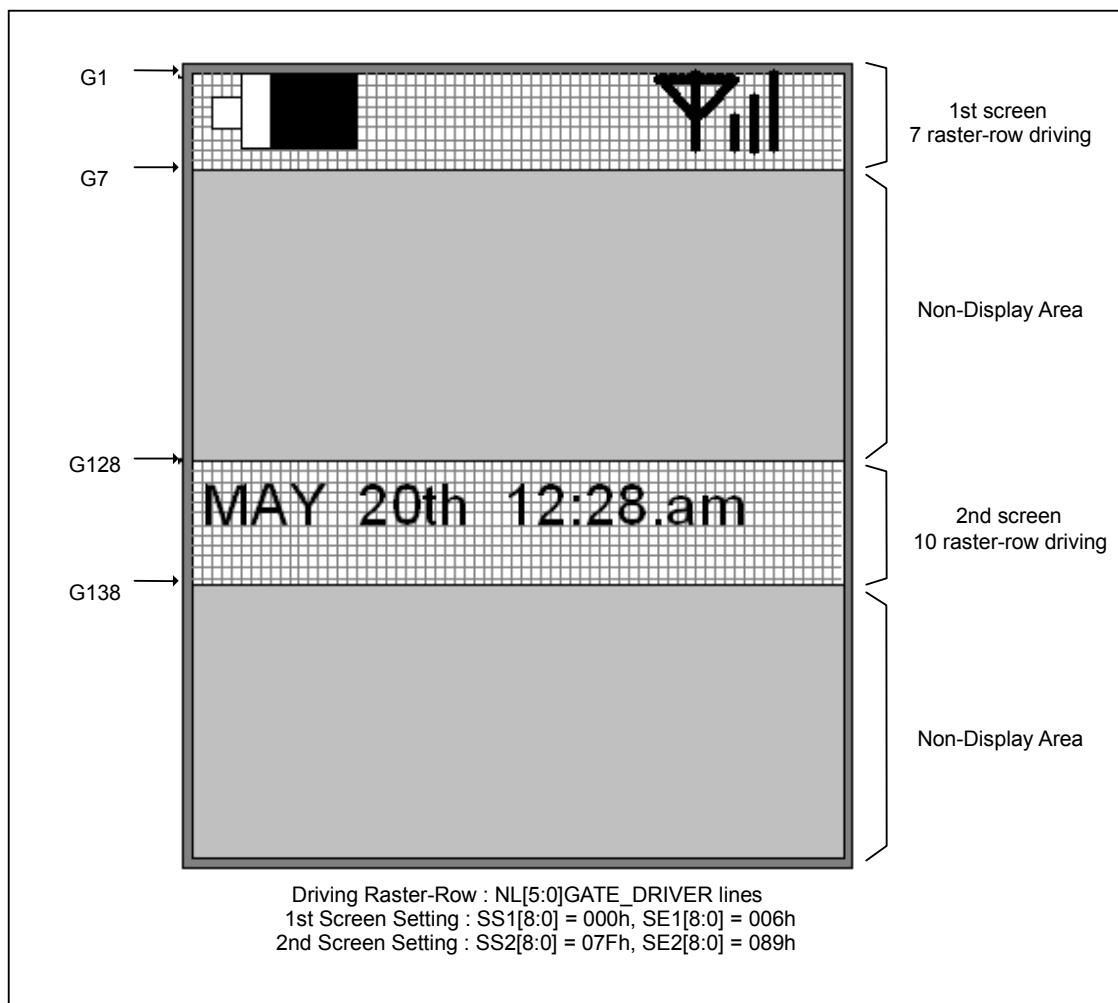


Figure 11-2 : Partial Display Mode

11.3. Partial Display Set-up

To specify partial display areas, the 1st screen area and the 2nd screen area should be defined.

For the 1st divided screen, start line and end line are specified by the 1st screen-driving position registers (SS1[8:0], SE1[8:0]).

For the 2nd divided screen, start line and end line are specified by the 2nd screen-driving position registers (SS2[8:0], SE2[8:0]).

Please make sure that the partial display area 1 and area 2 don't overlap each other.

Example of partial display set-up

Table 11-1 : Split Screen Driving Function with SPT = 0

Register value	Display Operation
$SE1[8:0] - SS1[8:0] = NL$	Full screen display Normally displays from SS1[8:0] to SE1[8:0]
$SE1[8:0] - SS1[8:0] < NL$	Partial display Normally displays from SS1[8:0] to SE1[8:0] Black or White display according to PT in remained area (DDRAM data is not related at all)
$SE1[8:0] - SS1[8:0] > NL$	Setting disabled

Table 11-2 : Split Screen Driving Function with SPT = 1

Register value	Display Operation
$SE1[8:0] - SS1[8:0] + SE2[8:0] - SS2[8:0] = NL$	Full screen display Normally displays from SS1[8:0] to SE2[8:0]
$SE1[8:0] - SS1[8:0] + SE2[8:0] - SS2[8:0] < NL$	Partial display Normally displays from SS1[8:0] to SE1[8:0] and from SS2[8:0] to SE2[8:0] Black or White display according to PT in remained area (DDRAM data is not related at all)
$SE1[8:0] - SS1[8:0] + SE2[8:0] - SS2[8:0] > NL$	Setting disabled

Refer to the following flowchart to set up Partial Display. It is possible to determine the output levels of the driver in Non-display area (the area out of partial display), so one can select appropriate level depending on the panel's condition.

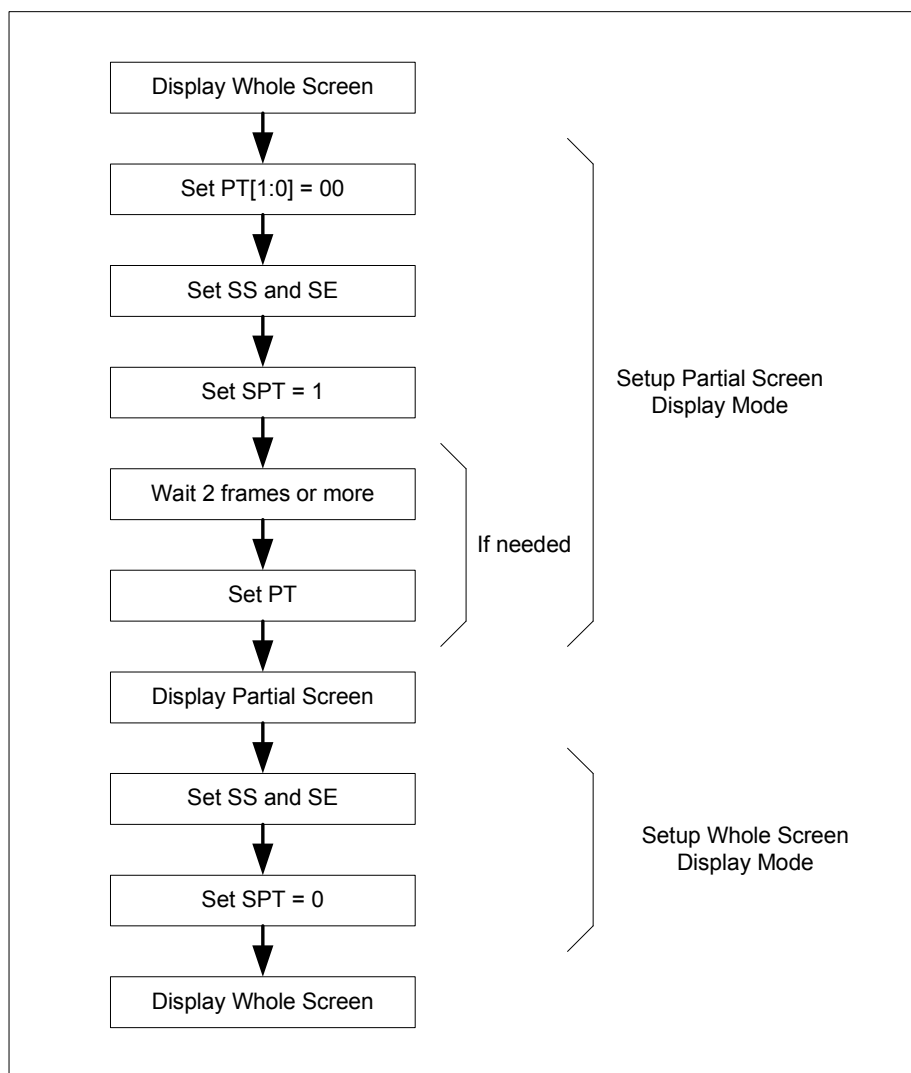


Figure 11-3 : Partial Display Setting Flow

12. Gamma Correction Function

The D51E5TA7601 has the gamma-correction function to display in 262,144 colors simultaneously. The gamma-correction is performed with 3 groups of registers (gradient adjustment, amplitude adjustment and fine adjustment registers) determining eight reference grayscale levels (VINP0-VINP7 or VINN0-VINN7). Each register group further consists of register groups of positive and negative polarities. Each register group is set independently to other register groups, making the D51E5TA7601 available with liquid crystal display panels of various characteristics.

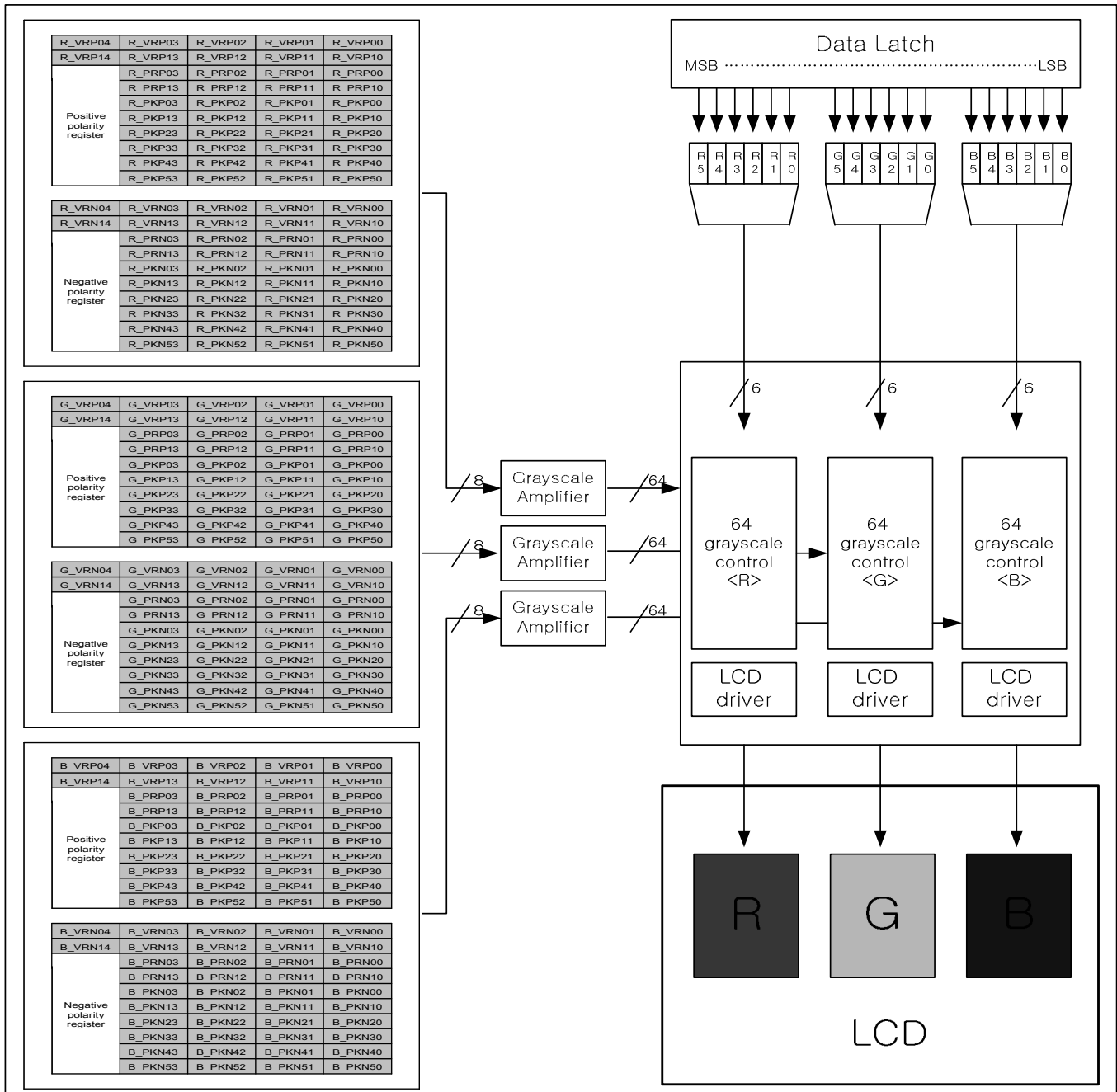


Figure 12-1 : Grayscale control

12.1. Structure of Grayscale Ladder

The figure below is the structure of a grayscale ladder. Eight levels (VINP0-VINP7, VINN0-VINN7) are specified by the amplitude adjustment registers, gradient adjustment and fine adjustment registers. Each voltage level is divided by the internal resistor ladder, and generates 64 levels. There are three grayscale ladders which are for Red, Green, and Blue.

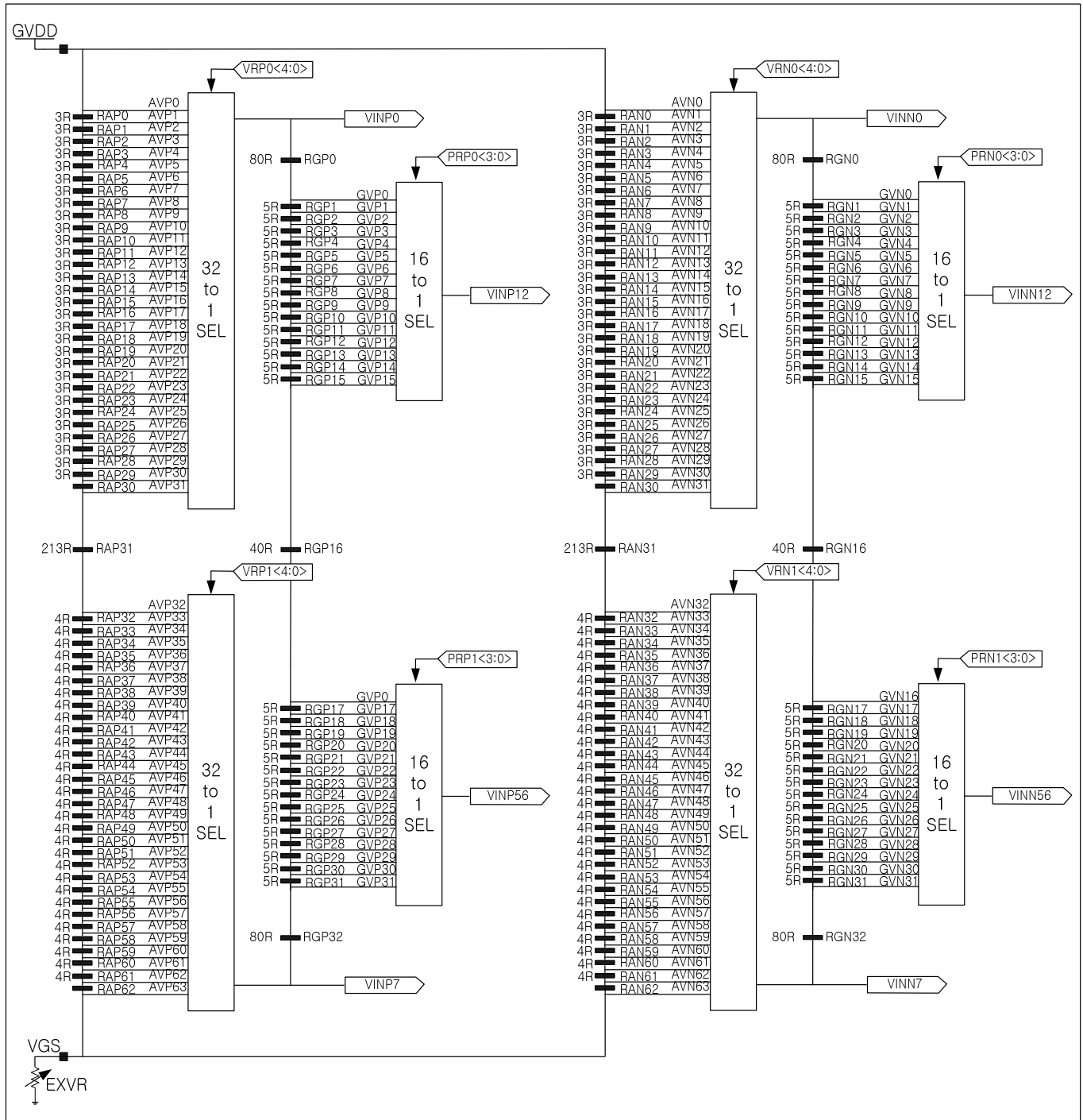


Figure 12-2 : Structure of Grayscale ladder Network 1

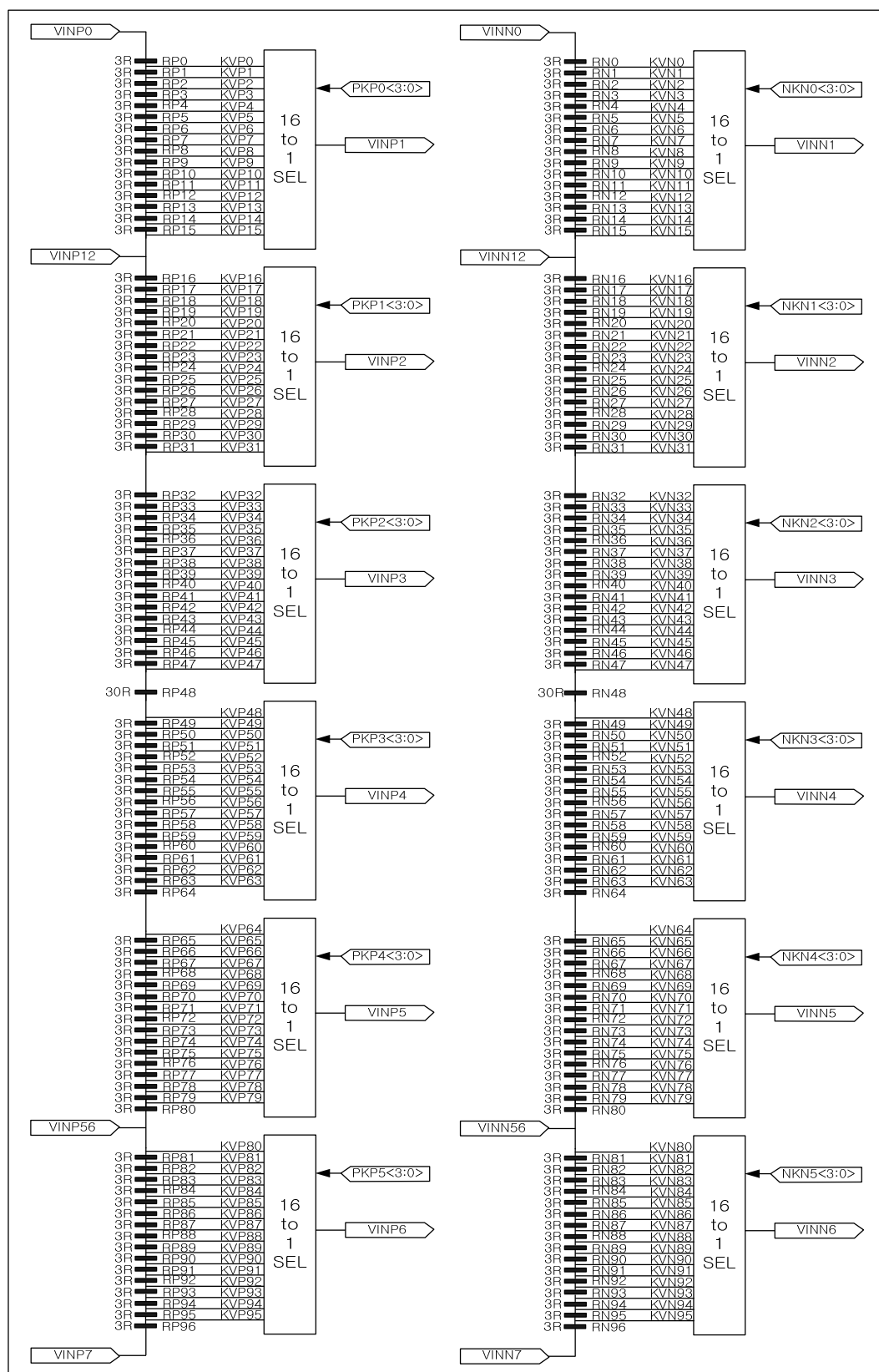


Figure 12-3 : Structure of Grayscale ladder Network 2

12.2. Grayscale Voltage Calculation Formula

The grayscale voltages V0 to V63 are specified when the internal ladder resistor is adjusted by the Gamma adjustment registers.

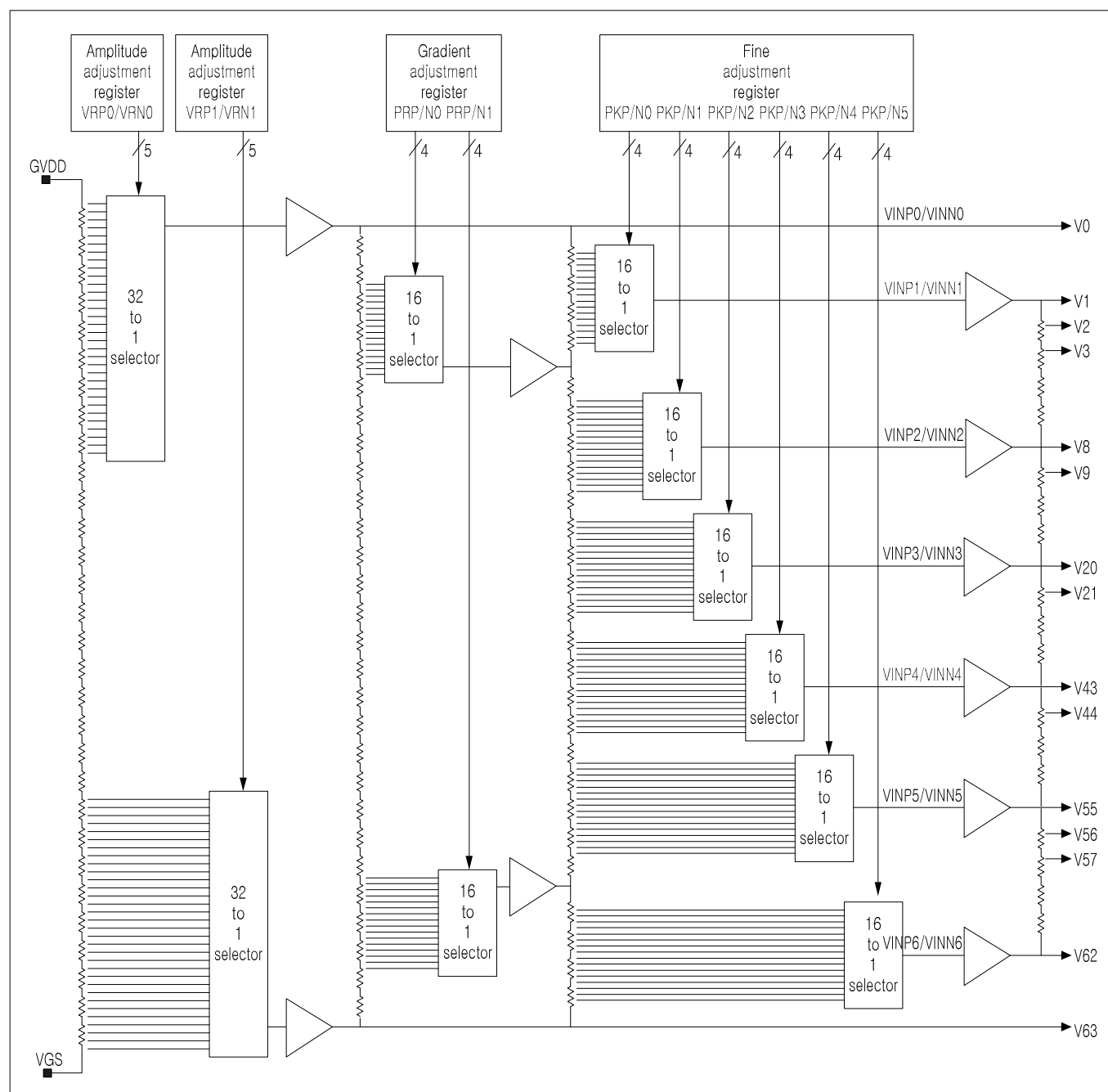


Figure 12-4 : Gamma curve correction circuit

12.3. Gamma Correction Registers

This block has register groups for specifying a grayscale voltage that meets the Gamma characteristics for the LCD panel used. These registers are divided into three groups, which correspond to the gradient, amplitude and fine adjustment of the grayscale characteristics for the voltage. The polarity of each register can be specified independently. (Red-Green-Blue Gamma can be adjusted individually.) The operations of the registers are described below.

Gradient adjustment

The gradient adjustment registers are used to adjust the gradient in the middle of the grayscale characteristics for the voltage without changing the dynamic range. (A : Gradient adjustment in the figure show below)

Amplitude adjustment

The amplitude adjustment registers are used to adjust the amplitude of the grayscale voltage. (B: Amplitude adjustment in the figure show below) This adjustment controls the values of the variable registers (VRP0/VRP1, VRN0/VRN1).

Fine adjustment

The fine adjustment register is to make subtle adjustment of the grayscale voltage level. (C: Fine adjustment in the figure show below)

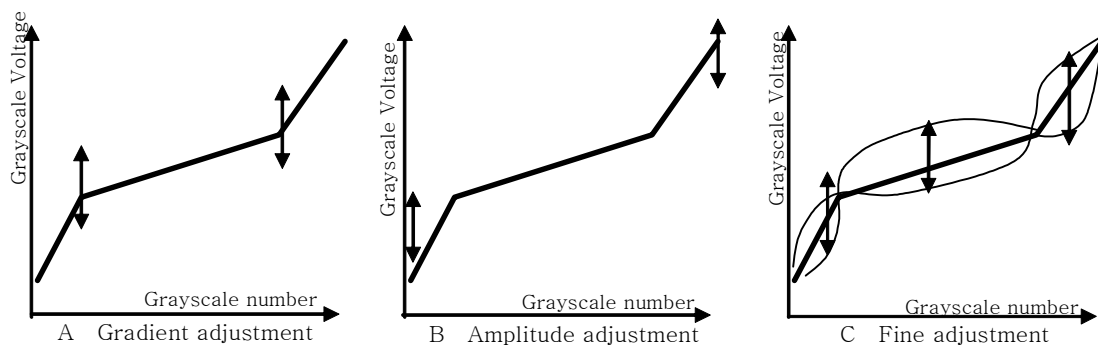


Figure 12-5 : Gamma correction curve

Gamma Adjustment Registers**Table 12-1 : Register control signal names**

Register Groups	Positive Polarity	Negative Polarity	Description
Gradient adjustment	R_PRP0 [3:0]	R_PRN0 [3:0]	16-to-1 selector (VINP12 / VINN12)
	G_PRP0 [3:0]	G_PRN0 [3:0]	
	B_PRP0 [3:0]	B_PRN0 [3:0]	
	R_PRP1 [3:0]	R_PRN1 [3:0]	16-to-1 selector (VINP56 / VINN56)
	G_PRP1 [3:0]	G_PRN1 [3:0]	
	B_PRP1 [3:0]	B_PRN1 [3:0]	
Amplitude adjustment	R_VRP0 [4:0]	R_VRN0 [4:0]	32-to-1 selector (VINP0 / VINN0)
	G_VRP0 [4:0]	G_VRN0 [4:0]	
	B_VRP0 [4:0]	B_VRN0 [4:0]	
	R_VRP1 [4:0]	R_VRN1 [4:0]	32-to-1 selector (VINP7 / VINN7)
	G_VRP1 [4:0]	G_VRN1 [4:0]	
	B_VRP1 [4:0]	B_VRN1 [4:0]	
Fine adjustment	R_PKP0 [3:0]	R_PKN0 [3:0]	16-to-1 selector (VINP1 / VINN1)
	G_PKP0 [3:0]	G_PKN0 [3:0]	
	B_PKP0 [3:0]	B_PKN0 [3:0]	
	R_PKP1 [3:0]	R_PKN1 [3:0]	16-to-1 selector (VINP2 / VINN2)
	G_PKP1 [3:0]	G_PKN1 [3:0]	
	B_PKP1 [3:0]	B_PKN1 [3:0]	
	R_PKP2 [3:0]	R_PKN2 [3:0]	16-to-1 selector (VINP3 / VINN3)
	G_PKP2 [3:0]	G_PKN2 [3:0]	
	B_PKP2 [3:0]	B_PKN2 [3:0]	
	R_PKP3 [3:0]	R_PKN3 [3:0]	16-to-1 selector (VINP4 / VINN4)
	G_PKP3 [3:0]	G_PKN3 [3:0]	
	B_PKP3 [3:0]	B_PKN3 [3:0]	
	R_PKP4 [3:0]	R_PKN4 [3:0]	16-to-1 selector (VINP5 / VINN5)
	G_PKP4 [3:0]	G_PKN4 [3:0]	
	B_PKP4 [3:0]	B_PKN4 [3:0]	
	R_PKP5 [3:0]	R_PKN5 [3:0]	16-to-1 selector (VINP6 / VINN6)
	G_PKP5 [3:0]	G_PKN5 [3:0]	
	B_PKP5 [3:0]	B_PKN5 [3:0]	

Resistor Ladder Network / Selectors

This block outputs the reference voltage of the grayscale voltage. There are three ladder resistors including the 32/16-to-1 selector selecting voltage generated by the resistor ladder. Also there are pins that connect to the external variable resistor. In addition, it allows compensating the dispersion of length between one panel and another.

(1) Resistor Ladder Network 1 / Selectors

There are 4 adjustments that are for the gradient adjustment (PRP(N)0/PRP(N)1) and for the amplitude adjustment (VRP(N)1/VRP(N)0). The voltage level is set by the gradient adjustment register and the amplitude adjustment registers as below.

Table 12-2 : Amplitude Adjustment (1)

VRP(N)0[4:0]	Selected Voltage VINP(N)0	Formula of VINP(N)0
00000	AVP(N)0	$(430R/430R) * (GVDD-VGS) + VGS$
00001	AVP(N)1	$(427R/430R) * (GVDD-VGS) + VGS$
00010	AVP(N)2	$(424R/430R) * (GVDD-VGS) + VGS$
00011	AVP(N)3	$(421R/430R) * (GVDD-VGS) + VGS$
00100	AVP(N)4	$(418R/430R) * (GVDD-VGS) + VGS$
00101	AVP(N)5	$(415R/430R) * (GVDD-VGS) + VGS$
00110	AVP(N)6	$(412R/430R) * (GVDD-VGS) + VGS$
00111	AVP(N)7	$(409R/430R) * (GVDD-VGS) + VGS$
01000	AVP(N)8	$(406R/430R) * (GVDD-VGS) + VGS$
01001	AVP(N)9	$(403R/430R) * (GVDD-VGS) + VGS$
01010	AVP(N)10	$(400R/430R) * (GVDD-VGS) + VGS$
01011	AVP(N)11	$(397R/430R) * (GVDD-VGS) + VGS$
01100	AVP(N)12	$(394R/430R) * (GVDD-VGS) + VGS$
01101	AVP(N)13	$(391R/430R) * (GVDD-VGS) + VGS$
01110	AVP(N)14	$(388R/430R) * (GVDD-VGS) + VGS$
01111	AVP(N)15	$(385R/430R) * (GVDD-VGS) + VGS$
10000	AVP(N)16	$(382R/430R) * (GVDD-VGS) + VGS$
10001	AVP(N)17	$(379R/430R) * (GVDD-VGS) + VGS$
10010	AVP(N)18	$(376R/430R) * (GVDD-VGS) + VGS$
10011	AVP(N)19	$(373R/430R) * (GVDD-VGS) + VGS$
10100	AVP(N)20	$(370R/430R) * (GVDD-VGS) + VGS$
10101	AVP(N)21	$(367R/430R) * (GVDD-VGS) + VGS$
10110	AVP(N)22	$(364R/430R) * (GVDD-VGS) + VGS$
10111	AVP(N)23	$(361R/430R) * (GVDD-VGS) + VGS$
11000	AVP(N)24	$(358R/430R) * (GVDD-VGS) + VGS$
11001	AVP(N)25	$(355R/430R) * (GVDD-VGS) + VGS$
11010	AVP(N)26	$(352R/430R) * (GVDD-VGS) + VGS$
11011	AVP(N)27	$(349R/430R) * (GVDD-VGS) + VGS$
11100	AVP(N)28	$(346R/430R) * (GVDD-VGS) + VGS$
11101	AVP(N)29	$(343R/430R) * (GVDD-VGS) + VGS$
11110	AVP(N)30	$(340R/430R) * (GVDD-VGS) + VGS$
11111	AVP(N)31	$(337R/430R) * (GVDD-VGS) + VGS$

Table 12-3 : Amplitude Adjustment (2)

VRP(N)1[4:0]	Selected Voltage VINP(N)7	Formula of VINP(N)0
00000	AVP(N)63	$(0R/430R) * (GVDD-VGS) + VGS$
00001	AVP(N)62	$(4R/430R) * (GVDD-VGS) + VGS$
00010	AVP(N)61	$(8R/430R) * (GVDD-VGS) + VGS$
00011	AVP(N)60	$(12R/430R) * (GVDD-VGS) + VGS$
00100	AVP(N)59	$(16R/430R) * (GVDD-VGS) + VGS$
00101	AVP(N)58	$(20R/430R) * (GVDD-VGS) + VGS$
00110	AVP(N)57	$(24R/430R) * (GVDD-VGS) + VGS$
00111	AVP(N)56	$(28R/430R) * (GVDD-VGS) + VGS$
01000	AVP(N)55	$(32R/430R) * (GVDD-VGS) + VGS$
01001	AVP(N)54	$(36R/430R) * (GVDD-VGS) + VGS$
01010	AVP(N)53	$(40R/430R) * (GVDD-VGS) + VGS$
01011	AVP(N)52	$(44R/430R) * (GVDD-VGS) + VGS$
01100	AVP(N)51	$(48R/430R) * (GVDD-VGS) + VGS$
01101	AVP(N)50	$(52R/430R) * (GVDD-VGS) + VGS$
01110	AVP(N)49	$(56R/430R) * (GVDD-VGS) + VGS$
01111	AVP(N)48	$(60R/430R) * (GVDD-VGS) + VGS$
10000	AVP(N)47	$(64R/430R) * (GVDD-VGS) + VGS$
10001	AVP(N)46	$(68R/430R) * (GVDD-VGS) + VGS$
10010	AVP(N)45	$(72R/430R) * (GVDD-VGS) + VGS$
10011	AVP(N)44	$(76R/430R) * (GVDD-VGS) + VGS$
10100	AVP(N)43	$(80R/430R) * (GVDD-VGS) + VGS$
10101	AVP(N)42	$(84R/430R) * (GVDD-VGS) + VGS$
10110	AVP(N)41	$(88R/430R) * (GVDD-VGS) + VGS$
10111	AVP(N)40	$(92R/430R) * (GVDD-VGS) + VGS$
11000	AVP(N)39	$(96R/430R) * (GVDD-VGS) + VGS$
11001	AVP(N)38	$(100R/430R) * (GVDD-VGS) + VGS$
11010	AVP(N)37	$(104R/430R) * (GVDD-VGS) + VGS$
11011	AVP(N)36	$(108R/430R) * (GVDD-VGS) + VGS$
11100	AVP(N)35	$(112R/430R) * (GVDD-VGS) + VGS$
11101	AVP(N)34	$(116R/430R) * (GVDD-VGS) + VGS$
11110	AVP(N)33	$(120R/430R) * (GVDD-VGS) + VGS$
11111	AVP(N)32	$(124R/430R) * (GVDD-VGS) + VGS$

Table 12-4 : Gradient Adjustment (1)

PRP(N)0[3:0]	Selected Voltage VINP(N)12	Formula of VINP(N)12
0000	GVP(N)0	$(270R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
0001	GVP(N)1	$(265R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
0010	GVP(N)2	$(260R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
0011	GVP(N)3	$(255R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
0100	GVP(N)4	$(250R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
0101	GVP(N)5	$(245R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
0110	GVP(N)6	$(240R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
0111	GVP(N)7	$(235R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
1000	GVP(N)8	$(230R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
1001	GVP(N)9	$(225R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
1010	GVP(N)10	$(220R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
1011	GVP(N)11	$(215R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
1100	GVP(N)12	$(210R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
1101	GVP(N)13	$(205R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
1110	GVP(N)14	$(200R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
1111	GVP(N)15	$(195R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$

Table 12-5 : Gradient Adjustment (2)

PRP(N)1[3:0]	Selected Voltage VINP(N)56	Formula of VINP(N)56
0000	GVP(N)31	$(80R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
0001	GVP(N)30	$(85R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
0010	GVP(N)29	$(90R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
0011	GVP(N)28	$(95R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
0100	GVP(N)27	$(100R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
0101	GVP(N)26	$(105R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
0110	GVP(N)25	$(110R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
0111	GVP(N)24	$(115R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
1000	GVP(N)23	$(120R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
1001	GVP(N)22	$(125R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
1010	GVP(N)21	$(130R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
1011	GVP(N)20	$(135R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
1100	GVP(N)19	$(140R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
1101	GVP(N)18	$(145R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
1110	GVP(N)17	$(150R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$
1111	GVP(N)16	$(155R/350R) * (VINP(N)0 - VINP(N)7) + VINP(N)7$

(2) Resistor Ladder Network 2 / Selectors

In the 16-to-1 selector, the voltage level must be selected by the given ladder resistance and the fine adjustment register and output the six types of the reference voltage, VIN1 to VIN6.

Table 12-6 : Fine Adjustment

Register values PKP(N)[3:0]	Selected voltage					
	VINP(N)1	VINP(N)2	VINP(N)3	VINP(N)4	VINP(N)5	VINP(N)6
0000	KVP(N)0	KVP(N)16	KVP(N)32	KVP(N)63	KVP(N)79	KVP(N)95
0001	KVP(N)1	KVP(N)17	KVP(N)33	KVP(N)62	KVP(N)78	KVP(N)94
0010	KVP(N)2	KVP(N)18	KVP(N)34	KVP(N)61	KVP(N)77	KVP(N)93
0011	KVP(N)3	KVP(N)19	KVP(N)35	KVP(N)60	KVP(N)76	KVP(N)92
0100	KVP(N)4	KVP(N)20	KVP(N)36	KVP(N)59	KVP(N)75	KVP(N)91
0101	KVP(N)5	KVP(N)21	KVP(N)37	KVP(N)58	KVP(N)74	KVP(N)90
0110	KVP(N)6	KVP(N)22	KVP(N)38	KVP(N)57	KVP(N)73	KVP(N)89
0111	KVP(N)7	KVP(N)23	KVP(N)39	KVP(N)56	KVP(N)72	KVP(N)88
1000	KVP(N)8	KVP(N)24	KVP(N)40	KVP(N)55	KVP(N)71	KVP(N)87
1001	KVP(N)9	KVP(N)25	KVP(N)41	KVP(N)54	KVP(N)70	KVP(N)86
1010	KVP(N)10	KVP(N)26	KVP(N)42	KVP(N)53	KVP(N)69	KVP(N)85
1011	KVP(N)11	KVP(N)27	KVP(N)43	KVP(N)52	KVP(N)68	KVP(N)84
1100	KVP(N)12	KVP(N)28	KVP(N)44	KVP(N)51	KVP(N)67	KVP(N)83
1101	KVP(N)13	KVP(N)29	KVP(N)45	KVP(N)50	KVP(N)66	KVP(N)82
1110	KVP(N)14	KVP(N)30	KVP(N)46	KVP(N)49	KVP(N)65	KVP(N)81
1111	KVP(N)15	KVP(N)31	KVP(N)47	KVP(N)48	KVP(N)64	KVP(N)80

The grayscale levels (V0-V63) for positive polarity are determined by the following formulas.

Voltage Calculation Formula (Positive polarity)

Table 12-7 : Gamma level calculation on positive polarity (1/3)

Pin	Formula	Fine adjustment register value	Reference voltage
KVP0	$(45R/48R) * (VINP0 - VINP12) + VINP12$	PKP0[3:0] = "0000"	VINP1
KVP1	$(42R/48R) * (VINP0 - VINP12) + VINP12$	PKP0[3:0] = "0001"	VINP1
KVP2	$(39R/48R) * (VINP0 - VINP12) + VINP12$	PKP0[3:0] = "0010"	VINP1
KVP3	$(36R/48R) * (VINP0 - VINP12) + VINP12$	PKP0[3:0] = "0011"	VINP1
KVP4	$(33R/48R) * (VINP0 - VINP12) + VINP12$	PKP0[3:0] = "0100"	VINP1
KVP5	$(30R/48R) * (VINP0 - VINP12) + VINP12$	PKP0[3:0] = "0101"	VINP1
KVP6	$(27R/48R) * (VINP0 - VINP12) + VINP12$	PKP0[3:0] = "0110"	VINP1
KVP7	$(24R/48R) * (VINP0 - VINP12) + VINP12$	PKP0[3:0] = "0111"	VINP1
KVP8	$(21R/48R) * (VINP0 - VINP12) + VINP12$	PKP0[3:0] = "1000"	VINP1
KVP9	$(18R/48R) * (VINP0 - VINP12) + VINP12$	PKP0[3:0] = "1001"	VINP1
KVP10	$(15R/48R) * (VINP0 - VINP12) + VINP12$	PKP0[3:0] = "1010"	VINP1
KVP11	$(12R/48R) * (VINP0 - VINP12) + VINP12$	PKP0[3:0] = "1011"	VINP1
KVP12	$(9R/48R) * (VINP0 - VINP12) + VINP12$	PKP0[3:0] = "1100"	VINP1
KVP13	$(6R/48R) * (VINP0 - VINP12) + VINP12$	PKP0[3:0] = "1101"	VINP1
KVP14	$(3R/48R) * (VINP0 - VINP12) + VINP12$	PKP0[3:0] = "1110"	VINP1
KVP15	VINP12	PKP0[3:0] = "1111"	VINP1
KVP16	$(219R/222R) * (VINP12 - VINP56) + VINP56$	PKP1[3:0] = "0000"	VINP2
KVP17	$(216R/222R) * (VINP12 - VINP56) + VINP56$	PKP1[3:0] = "0001"	VINP2
KVP18	$(213R/222R) * (VINP12 - VINP56) + VINP56$	PKP1[3:0] = "0010"	VINP2
KVP19	$(210R/222R) * (VINP12 - VINP56) + VINP56$	PKP1[3:0] = "0011"	VINP2
KVP20	$(207R/222R) * (VINP12 - VINP56) + VINP56$	PKP1[3:0] = "0100"	VINP2
KVP21	$(204R/222R) * (VINP12 - VINP56) + VINP56$	PKP1[3:0] = "0101"	VINP2
KVP22	$(201R/222R) * (VINP12 - VINP56) + VINP56$	PKP1[3:0] = "0110"	VINP2
KVP23	$(198R/222R) * (VINP12 - VINP56) + VINP56$	PKP1[3:0] = "0111"	VINP2
KVP24	$(195R/222R) * (VINP12 - VINP56) + VINP56$	PKP1[3:0] = "1000"	VINP2
KVP25	$(192R/222R) * (VINP12 - VINP56) + VINP56$	PKP1[3:0] = "1001"	VINP2
KVP26	$(189R/222R) * (VINP12 - VINP56) + VINP56$	PKP1[3:0] = "1010"	VINP2
KVP27	$(186R/222R) * (VINP12 - VINP56) + VINP56$	PKP1[3:0] = "1011"	VINP2
KVP28	$(183R/222R) * (VINP12 - VINP56) + VINP56$	PKP1[3:0] = "1100"	VINP2
KVP29	$(180R/222R) * (VINP12 - VINP56) + VINP56$	PKP1[3:0] = "1101"	VINP2
KVP30	$(177R/222R) * (VINP12 - VINP56) + VINP56$	PKP1[3:0] = "1110"	VINP2
KVP31	$(174R/222R) * (VINP12 - VINP56) + VINP56$	PKP1[3:0] = "1111"	VINP2
KVP32	$(171R/222R) * (VINP12 - VINP56) + VINP56$	PKP2[3:0] = "0000"	VINP3
KVP33	$(168R/222R) * (VINP12 - VINP56) + VINP56$	PKP2[3:0] = "0001"	VINP3
KVP34	$(165R/222R) * (VINP12 - VINP56) + VINP56$	PKP2[3:0] = "0010"	VINP3
KVP35	$(162R/222R) * (VINP12 - VINP56) + VINP56$	PKP2[3:0] = "0011"	VINP3
KVP36	$(159R/222R) * (VINP12 - VINP56) + VINP56$	PKP2[3:0] = "0100"	VINP3
KVP37	$(156R/222R) * (VINP12 - VINP56) + VINP56$	PKP2[3:0] = "0101"	VINP3
KVP38	$(153R/222R) * (VINP12 - VINP56) + VINP56$	PKP2[3:0] = "0110"	VINP3
KVP39	$(150R/222R) * (VINP12 - VINP56) + VINP56$	PKP2[3:0] = "0111"	VINP3
KVP40	$(147R/222R) * (VINP12 - VINP56) + VINP56$	PKP2[3:0] = "1000"	VINP3
KVP41	$(144R/222R) * (VINP12 - VINP56) + VINP56$	PKP2[3:0] = "1001"	VINP3
KVP42	$(141R/222R) * (VINP12 - VINP56) + VINP56$	PKP2[3:0] = "1010"	VINP3
KVP43	$(138R/222R) * (VINP12 - VINP56) + VINP56$	PKP2[3:0] = "1011"	VINP3
KVP44	$(135R/222R) * (VINP12 - VINP56) + VINP56$	PKP2[3:0] = "1100"	VINP3
KVP45	$(132R/222R) * (VINP12 - VINP56) + VINP56$	PKP2[3:0] = "1101"	VINP3
KVP46	$(129R/222R) * (VINP12 - VINP56) + VINP56$	PKP2[3:0] = "1110"	VINP3
KVP47	$(126R/222R) * (VINP12 - VINP56) + VINP56$	PKP2[3:0] = "1111"	VINP3

Table 12-8 : Gamma level calculation on positive polarity (2/3)

Pin	Formula	Fine adjustment register value	Reference voltage
KVP48	$(96R/222R) * (VINP12 - VINP56) + VINP56$	PKP3[3:0] = "0000"	VINP4
KVP49	$(93R/222R) * (VINP12 - VINP56) + VINP56$	PKP3[3:0] = "0001"	VINP4
KVP50	$(90R/222R) * (VINP12 - VINP56) + VINP56$	PKP3[3:0] = "0010"	VINP4
KVP51	$(87R/222R) * (VINP12 - VINP56) + VINP56$	PKP3[3:0] = "0011"	VINP4
KVP52	$(84R/222R) * (VINP12 - VINP56) + VINP56$	PKP3[3:0] = "0100"	VINP4
KVP53	$(81R/222R) * (VINP12 - VINP56) + VINP56$	PKP3[3:0] = "0101"	VINP4
KVP54	$(78R/222R) * (VINP12 - VINP56) + VINP56$	PKP3[3:0] = "0110"	VINP4
KVP55	$(75R/222R) * (VINP12 - VINP56) + VINP56$	PKP3[3:0] = "0111"	VINP4
KVP56	$(72R/222R) * (VINP12 - VINP56) + VINP56$	PKP3[3:0] = "1000"	VINP4
KVP57	$(69R/222R) * (VINP12 - VINP56) + VINP56$	PKP3[3:0] = "1001"	VINP4
KVP58	$(66R/222R) * (VINP12 - VINP56) + VINP56$	PKP3[3:0] = "1010"	VINP4
KVP59	$(63R/222R) * (VINP12 - VINP56) + VINP56$	PKP3[3:0] = "1011"	VINP4
KVP60	$(60R/222R) * (VINP12 - VINP56) + VINP56$	PKP3[3:0] = "1100"	VINP4
KVP61	$(57R/222R) * (VINP12 - VINP56) + VINP56$	PKP3[3:0] = "1101"	VINP4
KVP62	$(54R/222R) * (VINP12 - VINP56) + VINP56$	PKP3[3:0] = "1110"	VINP4
KVP63	$(51R/222R) * (VINP12 - VINP56) + VINP56$	PKP3[3:0] = "1111"	VINP4
KVP64	$(48R/222R) * (VINP12 - VINP56) + VINP56$	PKP4[3:0] = "0000"	VINP5
KVP65	$(45R/222R) * (VINP12 - VINP56) + VINP56$	PKP4[3:0] = "0001"	VINP5
KVP66	$(42R/222R) * (VINP12 - VINP56) + VINP56$	PKP4[3:0] = "0010"	VINP5
KVP67	$(39R/222R) * (VINP12 - VINP56) + VINP56$	PKP4[3:0] = "0011"	VINP5
KVP68	$(36R/222R) * (VINP12 - VINP56) + VINP56$	PKP4[3:0] = "0100"	VINP5
KVP69	$(33R/222R) * (VINP12 - VINP56) + VINP56$	PKP4[3:0] = "0101"	VINP5
KVP70	$(30R/222R) * (VINP12 - VINP56) + VINP56$	PKP4[3:0] = "0110"	VINP5
KVP71	$(27R/222R) * (VINP12 - VINP56) + VINP56$	PKP4[3:0] = "0111"	VINP5
KVP72	$(24R/222R) * (VINP12 - VINP56) + VINP56$	PKP4[3:0] = "1000"	VINP5
KVP73	$(21R/222R) * (VINP12 - VINP56) + VINP56$	PKP4[3:0] = "1001"	VINP5
KVP74	$(18R/222R) * (VINP12 - VINP56) + VINP56$	PKP4[3:0] = "1010"	VINP5
KVP75	$(15R/222R) * (VINP12 - VINP56) + VINP56$	PKP4[3:0] = "1011"	VINP5
KVP76	$(12R/222R) * (VINP12 - VINP56) + VINP56$	PKP4[3:0] = "1100"	VINP5
KVP77	$(9R/222R) * (VINP12 - VINP56) + VINP56$	PKP4[3:0] = "1101"	VINP5
KVP78	$(6R/222R) * (VINP12 - VINP56) + VINP56$	PKP4[3:0] = "1110"	VINP5
KVP79	$(3R/222R) * (VINP12 - VINP56) + VINP56$	PKP4[3:0] = "1111"	VINP5
KVP80	VINP56	PKP5[3:0] = "0000"	VINP6
KVP81	$(45R/48R) * (VINP56 - VINP7) + VINP7$	PKP5[3:0] = "0001"	VINP6
KVP82	$(42R/48R) * (VINP56 - VINP7) + VINP7$	PKP5[3:0] = "0010"	VINP6
KVP83	$(39R/48R) * (VINP56 - VINP7) + VINP7$	PKP5[3:0] = "0011"	VINP6
KVP84	$(36R/48R) * (VINP56 - VINP7) + VINP7$	PKP5[3:0] = "0100"	VINP6
KVP85	$(33R/48R) * (VINP56 - VINP7) + VINP7$	PKP5[3:0] = "0101"	VINP6
KVP86	$(30R/48R) * (VINP56 - VINP7) + VINP7$	PKP5[3:0] = "0110"	VINP6
KVP87	$(27R/48R) * (VINP56 - VINP7) + VINP7$	PKP5[3:0] = "0111"	VINP6
KVP88	$(24R/48R) * (VINP56 - VINP7) + VINP7$	PKP5[3:0] = "1000"	VINP6
KVP89	$(21R/48R) * (VINP56 - VINP7) + VINP7$	PKP5[3:0] = "1001"	VINP6
KVP90	$(18R/48R) * (VINP56 - VINP7) + VINP7$	PKP5[3:0] = "1010"	VINP6
KVP91	$(15R/48R) * (VINP56 - VINP7) + VINP7$	PKP5[3:0] = "1011"	VINP6
KVP92	$(12R/48R) * (VINP56 - VINP7) + VINP7$	PKP5[3:0] = "1100"	VINP6
KVP93	$(9R/48R) * (VINP56 - VINP7) + VINP7$	PKP5[3:0] = "1101"	VINP6
KVP94	$(6R/48R) * (VINP56 - VINP7) + VINP7$	PKP5[3:0] = "1110"	VINP6
KVP95	$(3R/48R) * (VINP56 - VINP7) + VINP7$	PKP5[3:0] = "1111"	VINP6

The grayscale levels (V0-V63) for positive polarity are determined by the following formulas.

Table 12-9 : Gamma level calculation on positive polarity (3/3)

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINP0	V32	$V20 - (V20 - V43) * (12 / 23)$
V1	VINP1	V33	$V20 - (V20 - V43) * (13 / 23)$
V2	$V1 - (V1 - V8) * (28 / 96)$	V34	$V20 - (V20 - V43) * (14 / 23)$
V3	$V1 - (V1 - V8) * (42 / 96)$	V35	$V20 - (V20 - V43) * (15 / 23)$
V4	$V1 - (V1 - V8) * (60 / 96)$	V36	$V20 - (V20 - V43) * (16 / 23)$
V5	$V1 - (V1 - V8) * (69 / 96)$	V37	$V20 - (V20 - V43) * (17 / 23)$
V6	$V1 - (V1 - V8) * (78 / 96)$	V38	$V20 - (V20 - V43) * (18 / 23)$
V7	$V1 - (V1 - V8) * (87 / 96)$	V39	$V20 - (V20 - V43) * (19 / 23)$
V8	VINP2	V40	$V20 - (V20 - V43) * (20 / 23)$
V9	$V8 - (V8 - V20) * (2 / 24)$	V41	$V20 - (V20 - V43) * (21 / 23)$
V10	$V8 - (V8 - V20) * (4 / 24)$	V42	$V20 - (V20 - V43) * (22 / 23)$
V11	$V8 - (V8 - V20) * (6 / 24)$	V43	VINP4
V12	$V8 - (V8 - V20) * (8 / 24)$	V44	$V43 - (V43 - V55) * (2 / 24)$
V13	$V8 - (V8 - V20) * (10 / 24)$	V45	$V43 - (V43 - V55) * (4 / 24)$
V14	$V8 - (V8 - V20) * (12 / 24)$	V46	$V43 - (V43 - V55) * (6 / 24)$
V15	$V8 - (V8 - V20) * (14 / 24)$	V47	$V43 - (V43 - V55) * (8 / 24)$
V16	$V8 - (V8 - V20) * (16 / 24)$	V48	$V43 - (V43 - V55) * (10 / 24)$
V17	$V8 - (V8 - V20) * (18 / 24)$	V49	$V43 - (V43 - V55) * (12 / 24)$
V18	$V8 - (V8 - V20) * (20 / 24)$	V50	$V43 - (V43 - V55) * (14 / 24)$
V19	$V8 - (V8 - V20) * (22 / 24)$	V51	$V43 - (V43 - V55) * (16 / 24)$
V20	VINP3	V52	$V43 - (V43 - V55) * (18 / 24)$
V21	$V20 - (V20 - V43) * (1 / 23)$	V53	$V43 - (V43 - V55) * (20 / 24)$
V22	$V20 - (V20 - V43) * (2 / 23)$	V54	$V43 - (V43 - V55) * (22 / 24)$
V23	$V20 - (V20 - V43) * (3 / 23)$	V55	VINP5
V24	$V20 - (V20 - V43) * (4 / 23)$	V56	$V55 - (V55 - V62) * (9 / 96)$
V25	$V20 - (V20 - V43) * (5 / 23)$	V57	$V55 - (V55 - V62) * (18 / 96)$
V26	$V20 - (V20 - V43) * (6 / 23)$	V58	$V55 - (V55 - V62) * (27 / 96)$
V27	$V20 - (V20 - V43) * (7 / 23)$	V59	$V55 - (V55 - V62) * (36 / 96)$
V28	$V20 - (V20 - V43) * (8 / 23)$	V60	$V55 - (V55 - V62) * (54 / 96)$
V29	$V20 - (V20 - V43) * (9 / 23)$	V61	$V55 - (V55 - V62) * (68 / 96)$
V30	$V20 - (V20 - V43) * (10 / 23)$	V62	VINP6
V31	$V20 - (V20 - V43) * (11 / 23)$	V63	VINP7

The grayscale levels (V0-V63) for negative polarity are determined by the following formulas.

Voltage Calculation Formula (Negative polarity)

Table 12-10 : Gamma level calculation on negative polarity (1/3)

Pin	Formula	Fine adjustment register value	Reference voltage
KVN0	$(45R/48R) * (VINN0 - VINN12) + VINN12$	PKN0[3:0] = "0000"	VINN1
KVN1	$(42R/48R) * (VINN0 - VINN12) + VINN12$	PKN0[3:0] = "0001"	VINN1
KVN2	$(39R/48R) * (VINN0 - VINN12) + VINN12$	PKN0[3:0] = "0010"	VINN1
KVN3	$(36R/48R) * (VINN0 - VINN12) + VINN12$	PKN0[3:0] = "0011"	VINN1
KVN4	$(33R/48R) * (VINN0 - VINN12) + VINN12$	PKN0[3:0] = "0100"	VINN1
KVN5	$(30R/48R) * (VINN0 - VINN12) + VINN12$	PKN0[3:0] = "0101"	VINN1
KVN6	$(27R/48R) * (VINN0 - VINN12) + VINN12$	PKN0[3:0] = "0110"	VINN1
KVN7	$(24R/48R) * (VINN0 - VINN12) + VINN12$	PKN0[3:0] = "0111"	VINN1
KVN8	$(21R/48R) * (VINN0 - VINN12) + VINN12$	PKN0[3:0] = "1000"	VINN1
KVN9	$(18R/48R) * (VINN0 - VINN12) + VINN12$	PKN0[3:0] = "1001"	VINN1
KVN10	$(15R/48R) * (VINN0 - VINN12) + VINN12$	PKN0[3:0] = "1010"	VINN1
KVN11	$(12R/48R) * (VINN0 - VINN12) + VINN12$	PKN0[3:0] = "1011"	VINN1
KVN12	$(9R/48R) * (VINN0 - VINN12) + VINN12$	PKN0[3:0] = "1100"	VINN1
KVN13	$(6R/48R) * (VINN0 - VINN12) + VINN12$	PKN0[3:0] = "1101"	VINN1
KVN14	$(3R/48R) * (VINN0 - VINN12) + VINN12$	PKN0[3:0] = "1110"	VINN1
KVN15	VINN12	PKN0[3:0] = "1111"	VINN1
KVN16	$(219R/222R) * (VINN12 - VINN56) + VINN56$	PKN1[3:0] = "0000"	VINN2
KVN17	$(216R/222R) * (VINN12 - VINN56) + VINN56$	PKN1[3:0] = "0001"	VINN2
KVN18	$(213R/222R) * (VINN12 - VINN56) + VINN56$	PKN1[3:0] = "0010"	VINN2
KVN19	$(210R/222R) * (VINN12 - VINN56) + VINN56$	PKN1[3:0] = "0011"	VINN2
KVN20	$(207R/222R) * (VINN12 - VINN56) + VINN56$	PKN1[3:0] = "0100"	VINN2
KVN21	$(204R/222R) * (VINN12 - VINN56) + VINN56$	PKN1[3:0] = "0101"	VINN2
KVN22	$(201R/222R) * (VINN12 - VINN56) + VINN56$	PKN1[3:0] = "0110"	VINN2
KVN23	$(198R/222R) * (VINN12 - VINN56) + VINN56$	PKN1[3:0] = "0111"	VINN2
KVN24	$(195R/222R) * (VINN12 - VINN56) + VINN56$	PKN1[3:0] = "1000"	VINN2
KVN25	$(192R/222R) * (VINN12 - VINN56) + VINN56$	PKN1[3:0] = "1001"	VINN2
KVN26	$(189R/222R) * (VINN12 - VINN56) + VINN56$	PKN1[3:0] = "1010"	VINN2
KVN27	$(186R/222R) * (VINN12 - VINN56) + VINN56$	PKN1[3:0] = "1011"	VINN2
KVN28	$(183R/222R) * (VINN12 - VINN56) + VINN56$	PKN1[3:0] = "1100"	VINN2
KVN29	$(180R/222R) * (VINN12 - VINN56) + VINN56$	PKN1[3:0] = "1101"	VINN2
KVN30	$(177R/222R) * (VINN12 - VINN56) + VINN56$	PKN1[3:0] = "1110"	VINN2
KVN31	$(174R/222R) * (VINN12 - VINN56) + VINN56$	PKN1[3:0] = "1111"	VINN2
KVN32	$(171R/222R) * (VINN12 - VINN56) + VINN56$	PKN2[3:0] = "0000"	VINN3
KVN33	$(168R/222R) * (VINN12 - VINN56) + VINN56$	PKN2[3:0] = "0001"	VINN3
KVN34	$(165R/222R) * (VINN12 - VINN56) + VINN56$	PKN2[3:0] = "0010"	VINN3
KVN35	$(162R/222R) * (VINN12 - VINN56) + VINN56$	PKN2[3:0] = "0011"	VINN3
KVN36	$(159R/222R) * (VINN12 - VINN56) + VINN56$	PKN2[3:0] = "0100"	VINN3
KVN37	$(156R/222R) * (VINN12 - VINN56) + VINN56$	PKN2[3:0] = "0101"	VINN3
KVN38	$(153R/222R) * (VINN12 - VINN56) + VINN56$	PKN2[3:0] = "0110"	VINN3
KVN39	$(150R/222R) * (VINN12 - VINN56) + VINN56$	PKN2[3:0] = "0111"	VINN3
KVN40	$(147R/222R) * (VINN12 - VINN56) + VINN56$	PKN2[3:0] = "1000"	VINN3
KVN41	$(144R/222R) * (VINN12 - VINN56) + VINN56$	PKN2[3:0] = "1001"	VINN3
KVN42	$(141R/222R) * (VINN12 - VINN56) + VINN56$	PKN2[3:0] = "1010"	VINN3
KVN43	$(138R/222R) * (VINN12 - VINN56) + VINN56$	PKN2[3:0] = "1011"	VINN3
KVN44	$(135R/222R) * (VINN12 - VINN56) + VINN56$	PKN2[3:0] = "1100"	VINN3
KVN45	$(132R/222R) * (VINN12 - VINN56) + VINN56$	PKN2[3:0] = "1101"	VINN3
KVN46	$(129R/222R) * (VINN12 - VINN56) + VINN56$	PKN2[3:0] = "1110"	VINN3
KVN47	$(126R/222R) * (VINN12 - VINN56) + VINN56$	PKN2[3:0] = "1111"	VINN3

Table 12-11 : Gamma level calculation on negative polarity (2/3)

Pin	Formula	Fine adjustment register value	Reference voltage
KVN48	$(96R/222R) * (VINN12 - VINN56) + VINN56$	PKN3[3:0] = "0000"	VINN4
KVN49	$(93R/222R) * (VINN12 - VINN56) + VINN56$	PKN3[3:0] = "0001"	VINN4
KVN50	$(90R/222R) * (VINN12 - VINN56) + VINN56$	PKN3[3:0] = "0010"	VINN4
KVN51	$(87R/222R) * (VINN12 - VINN56) + VINN56$	PKN3[3:0] = "0011"	VINN4
KVN52	$(84R/222R) * (VINN12 - VINN56) + VINN56$	PKN3[3:0] = "0100"	VINN4
KVN53	$(81R/222R) * (VINN12 - VINN56) + VINN56$	PKN3[3:0] = "0101"	VINN4
KVN54	$(78R/222R) * (VINN12 - VINN56) + VINN56$	PKN3[3:0] = "0110"	VINN4
KVN55	$(75R/222R) * (VINN12 - VINN56) + VINN56$	PKN3[3:0] = "0111"	VINN4
KVN56	$(72R/222R) * (VINN12 - VINN56) + VINN56$	PKN3[3:0] = "1000"	VINN4
KVN57	$(69R/222R) * (VINN12 - VINN56) + VINN56$	PKN3[3:0] = "1001"	VINN4
KVN58	$(66R/222R) * (VINN12 - VINN56) + VINN56$	PKN3[3:0] = "1010"	VINN4
KVN59	$(63R/222R) * (VINN12 - VINN56) + VINN56$	PKN3[3:0] = "1011"	VINN4
KVN60	$(60R/222R) * (VINN12 - VINN56) + VINN56$	PKN3[3:0] = "1100"	VINN4
KVN61	$(57R/222R) * (VINN12 - VINN56) + VINN56$	PKN3[3:0] = "1101"	VINN4
KVN62	$(54R/222R) * (VINN12 - VINN56) + VINN56$	PKN3[3:0] = "1110"	VINN4
KVN63	$(51R/222R) * (VINN12 - VINN56) + VINN56$	PKN3[3:0] = "1111"	VINN4
KVN64	$(48R/222R) * (VINN12 - VINN56) + VINN56$	PKN4[3:0] = "0000"	VINN5
KVN65	$(45R/222R) * (VINN12 - VINN56) + VINN56$	PKN4[3:0] = "0001"	VINN5
KVN66	$(42R/222R) * (VINN12 - VINN56) + VINN56$	PKN4[3:0] = "0010"	VINN5
KVN67	$(39R/222R) * (VINN12 - VINN56) + VINN56$	PKN4[3:0] = "0011"	VINN5
KVN68	$(36R/222R) * (VINN12 - VINN56) + VINN56$	PKN4[3:0] = "0100"	VINN5
KVN69	$(33R/222R) * (VINN12 - VINN56) + VINN56$	PKN4[3:0] = "0101"	VINN5
KVN70	$(30R/222R) * (VINN12 - VINN56) + VINN56$	PKN4[3:0] = "0110"	VINN5
KVN71	$(27R/222R) * (VINN12 - VINN56) + VINN56$	PKN4[3:0] = "0111"	VINN5
KVN72	$(24R/222R) * (VINN12 - VINN56) + VINN56$	PKN4[3:0] = "1000"	VINN5
KVN73	$(21R/222R) * (VINN12 - VINN56) + VINN56$	PKN4[3:0] = "1001"	VINN5
KVN74	$(18R/222R) * (VINN12 - VINN56) + VINN56$	PKN4[3:0] = "1010"	VINN5
KVN75	$(15R/222R) * (VINN12 - VINN56) + VINN56$	PKN4[3:0] = "1011"	VINN5
KVN76	$(12R/222R) * (VINN12 - VINN56) + VINN56$	PKN4[3:0] = "1100"	VINN5
KVN77	$(9R/222R) * (VINN12 - VINN56) + VINN56$	PKN4[3:0] = "1101"	VINN5
KVN78	$(6R/222R) * (VINN12 - VINN56) + VINN56$	PKN4[3:0] = "1110"	VINN5
KVN79	$(3R/222R) * (VINN12 - VINN56) + VINN56$	PKN4[3:0] = "1111"	VINN5
KVN80	VINN56	PKN5[3:0] = "0000"	VINN6
KVN81	$(45R/48R) * (VINN56 - VINN7) + VINN7$	PKN5[3:0] = "0001"	VINN6
KVN82	$(42R/48R) * (VINN56 - VINN7) + VINN7$	PKN5[3:0] = "0010"	VINN6
KVN83	$(39R/48R) * (VINN56 - VINN7) + VINN7$	PKN5[3:0] = "0011"	VINN6
KVN84	$(36R/48R) * (VINN56 - VINN7) + VINN7$	PKN5[3:0] = "0100"	VINN6
KVN85	$(33R/48R) * (VINN56 - VINN7) + VINN7$	PKN5[3:0] = "0101"	VINN6
KVN86	$(30R/48R) * (VINN56 - VINN7) + VINN7$	PKN5[3:0] = "0110"	VINN6
KVN87	$(27R/48R) * (VINN56 - VINN7) + VINN7$	PKN5[3:0] = "0111"	VINN6
KVN88	$(24R/48R) * (VINN56 - VINN7) + VINN7$	PKN5[3:0] = "1000"	VINN6
KVN89	$(21R/48R) * (VINN56 - VINN7) + VINN7$	PKN5[3:0] = "1001"	VINN6
KVN90	$(18R/48R) * (VINN56 - VINN7) + VINN7$	PKN5[3:0] = "1010"	VINN6
KVN91	$(15R/48R) * (VINN56 - VINN7) + VINN7$	PKN5[3:0] = "1011"	VINN6
KVN92	$(12R/48R) * (VINN56 - VINN7) + VINN7$	PKN5[3:0] = "1100"	VINN6
KVN93	$(9R/48R) * (VINN56 - VINN7) + VINN7$	PKN5[3:0] = "1101"	VINN6
KVN94	$(6R/48R) * (VINN56 - VINN7) + VINN7$	PKN5[3:0] = "1110"	VINN6
KVN95	$(3R/48R) * (VINN56 - VINN7) + VINN7$	PKN5[3:0] = "1111"	VINN6

The grayscale levels (V0-V63) for negative polarity are determined by the following formulas.

Table 12-12 : Gamma level calculation on negative polarity (3/3)

Grayscale voltage	Formula	Grayscale voltage	Formula
V0	VINN0	V32	$V20 - (V20 - V43) * (12 / 23)$
V1	VINN1	V33	$V20 - (V20 - V43) * (13 / 23)$
V2	$V1 - (V1 - V8) * (28 / 96)$	V34	$V20 - (V20 - V43) * (14 / 23)$
V3	$V1 - (V1 - V8) * (42 / 96)$	V35	$V20 - (V20 - V43) * (15 / 23)$
V4	$V1 - (V1 - V8) * (60 / 96)$	V36	$V20 - (V20 - V43) * (16 / 23)$
V5	$V1 - (V1 - V8) * (69 / 96)$	V37	$V20 - (V20 - V43) * (17 / 23)$
V6	$V1 - (V1 - V8) * (78 / 96)$	V38	$V20 - (V20 - V43) * (18 / 23)$
V7	$V1 - (V1 - V8) * (87 / 96)$	V39	$V20 - (V20 - V43) * (19 / 23)$
V8	VINN2	V40	$V20 - (V20 - V43) * (20 / 23)$
V9	$V8 - (V8 - V20) * (2 / 24)$	V41	$V20 - (V20 - V43) * (21 / 23)$
V10	$V8 - (V8 - V20) * (4 / 24)$	V42	$V20 - (V20 - V43) * (22 / 23)$
V11	$V8 - (V8 - V20) * (6 / 24)$	V43	VINN4
V12	$V8 - (V8 - V20) * (8 / 24)$	V44	$V43 - (V43 - V55) * (2 / 24)$
V13	$V8 - (V8 - V20) * (10 / 24)$	V45	$V43 - (V43 - V55) * (4 / 24)$
V14	$V8 - (V8 - V20) * (12 / 24)$	V46	$V43 - (V43 - V55) * (6 / 24)$
V15	$V8 - (V8 - V20) * (14 / 24)$	V47	$V43 - (V43 - V55) * (8 / 24)$
V16	$V8 - (V8 - V20) * (16 / 24)$	V48	$V43 - (V43 - V55) * (10 / 24)$
V17	$V8 - (V8 - V20) * (18 / 24)$	V49	$V43 - (V43 - V55) * (12 / 24)$
V18	$V8 - (V8 - V20) * (20 / 24)$	V50	$V43 - (V43 - V55) * (14 / 24)$
V19	$V8 - (V8 - V20) * (22 / 24)$	V51	$V43 - (V43 - V55) * (16 / 24)$
V20	VINN3	V52	$V43 - (V43 - V55) * (18 / 24)$
V21	$V20 - (V20 - V43) * (1 / 23)$	V53	$V43 - (V43 - V55) * (20 / 24)$
V22	$V20 - (V20 - V43) * (2 / 23)$	V54	$V43 - (V43 - V55) * (22 / 24)$
V23	$V20 - (V20 - V43) * (3 / 23)$	V55	VINN5
V24	$V20 - (V20 - V43) * (4 / 23)$	V56	$V55 - (V55 - V62) * (9 / 96)$
V25	$V20 - (V20 - V43) * (5 / 23)$	V57	$V55 - (V55 - V62) * (18 / 96)$
V26	$V20 - (V20 - V43) * (6 / 23)$	V58	$V55 - (V55 - V62) * (27 / 96)$
V27	$V20 - (V20 - V43) * (7 / 23)$	V59	$V55 - (V55 - V62) * (36 / 96)$
V28	$V20 - (V20 - V43) * (8 / 23)$	V60	$V55 - (V55 - V62) * (54 / 96)$
V29	$V20 - (V20 - V43) * (9 / 23)$	V61	$V55 - (V55 - V62) * (68 / 96)$
V30	$V20 - (V20 - V43) * (10 / 23)$	V62	VINN6
V31	$V20 - (V20 - V43) * (11 / 23)$	V63	VINN7

12.4. The Relation between Grayscale Voltage and Display Data

The relation between the DDRAM data and output level is shown in the figures below.

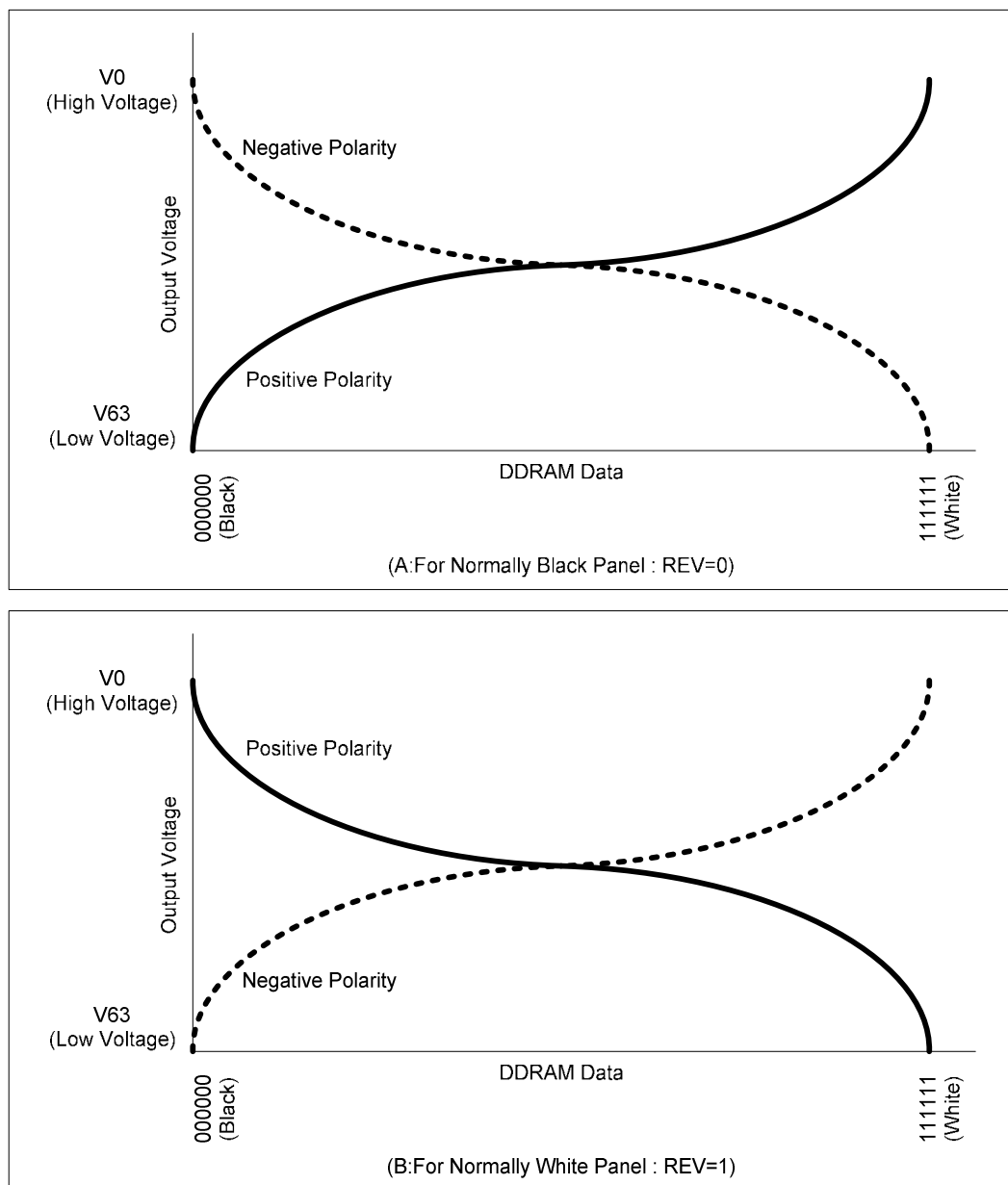


Figure 12-6 : Source Output Control with DDRAM data according to polarity

13. Display Setup Sequence

13.1. Power-On Sequence (Auto Sequence. APON = "H")

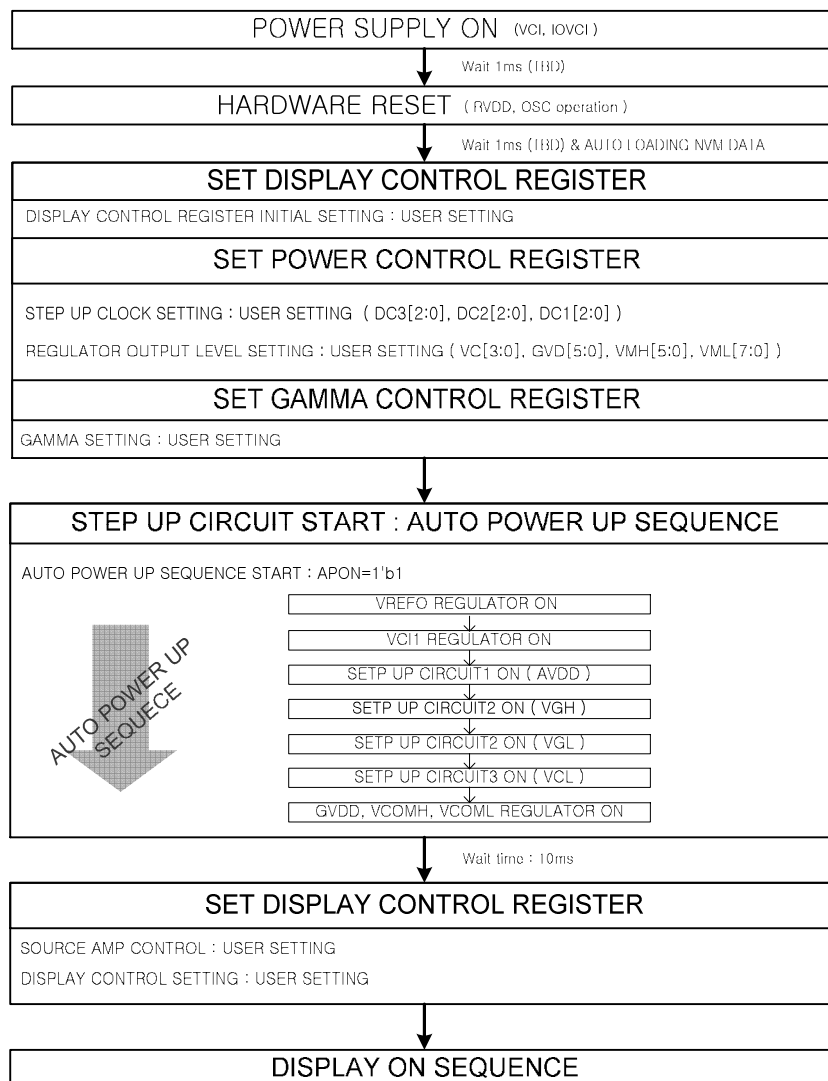


Figure 13-1 : Auto Power On Sequence

13.2. Power-On Sequence (Manual Boosting Sequence. APON = “L”)

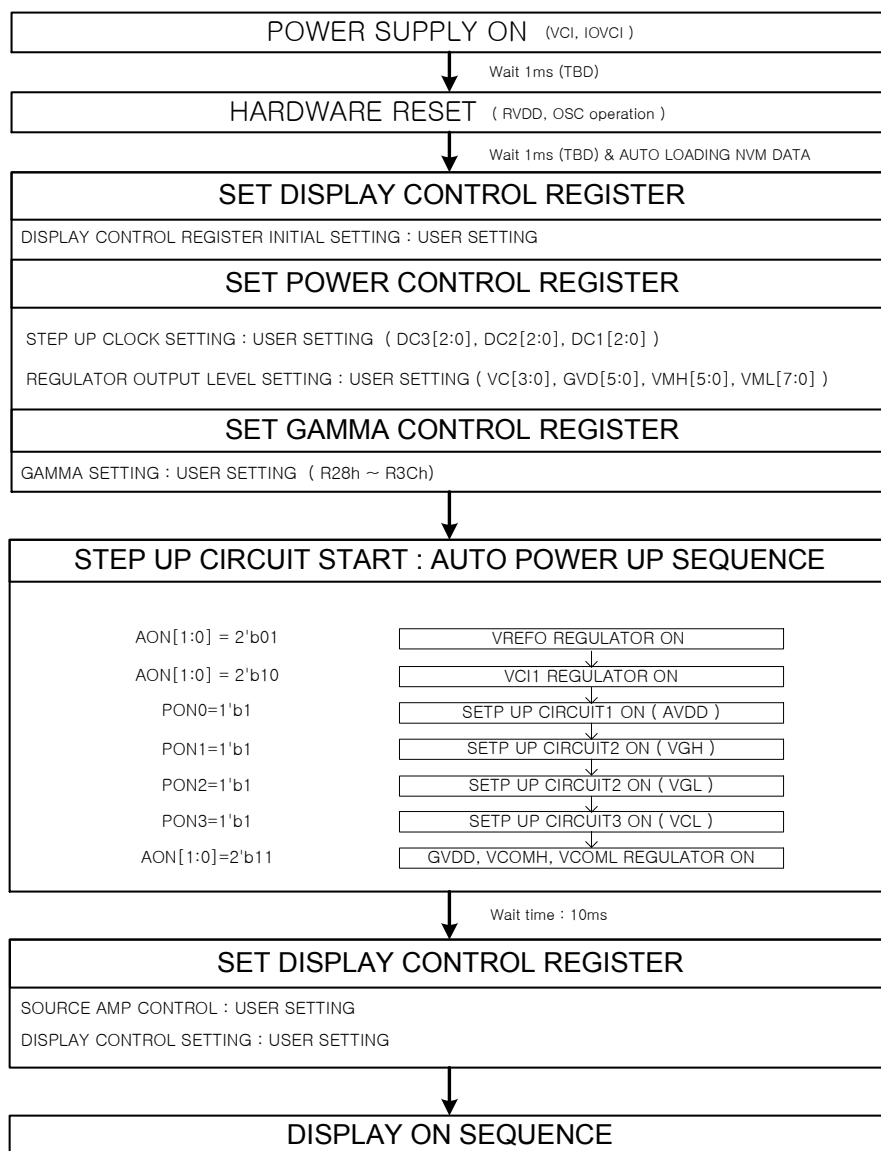


Figure 13-2 : Manual Power On Sequence

13.3. Power OFF Sequence

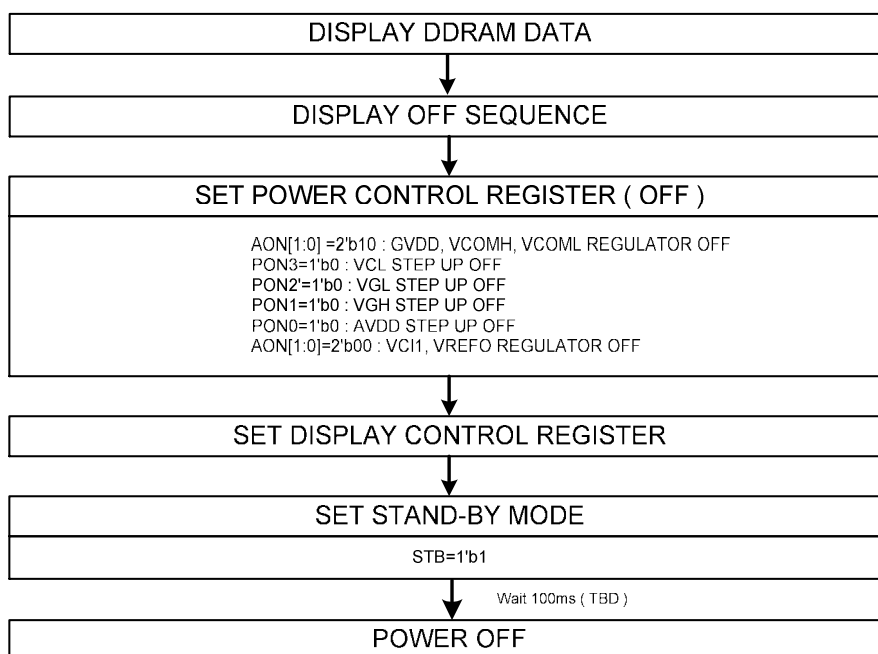


Figure 13-3 : Power Off Sequence

13.4. Display ON Sequence

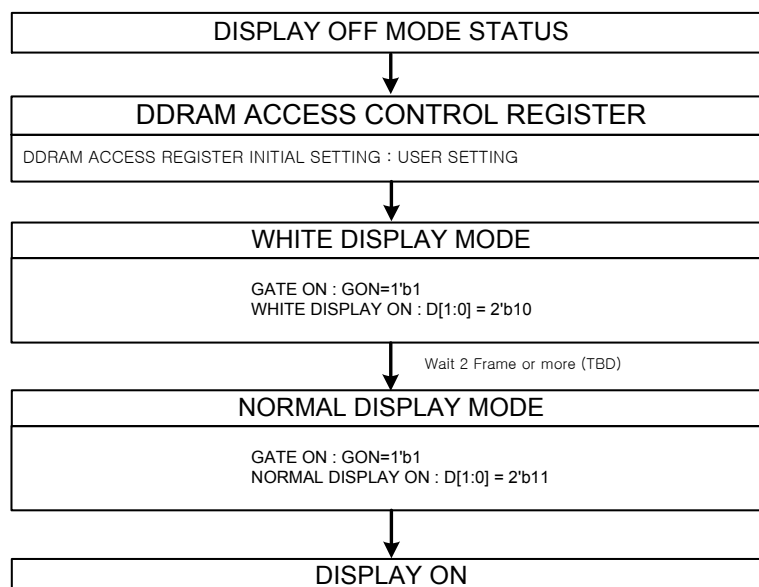


Figure 13-4 : Display On Sequence

13.5. Display OFF Sequence

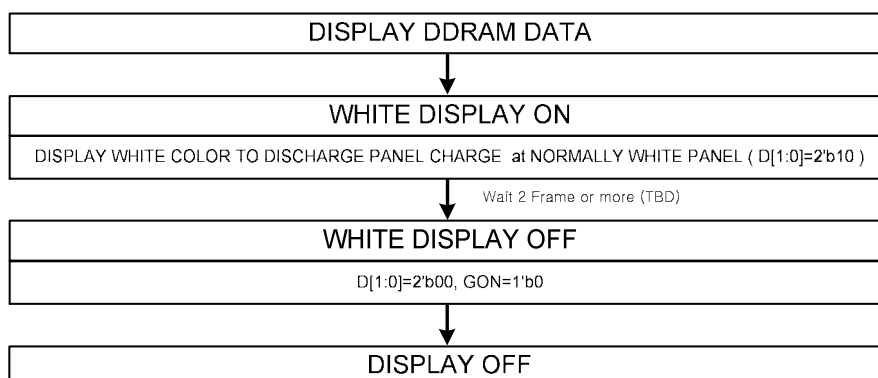


Figure 13-5 : Display Off Sequence

13.6. Stand-by IN Sequence

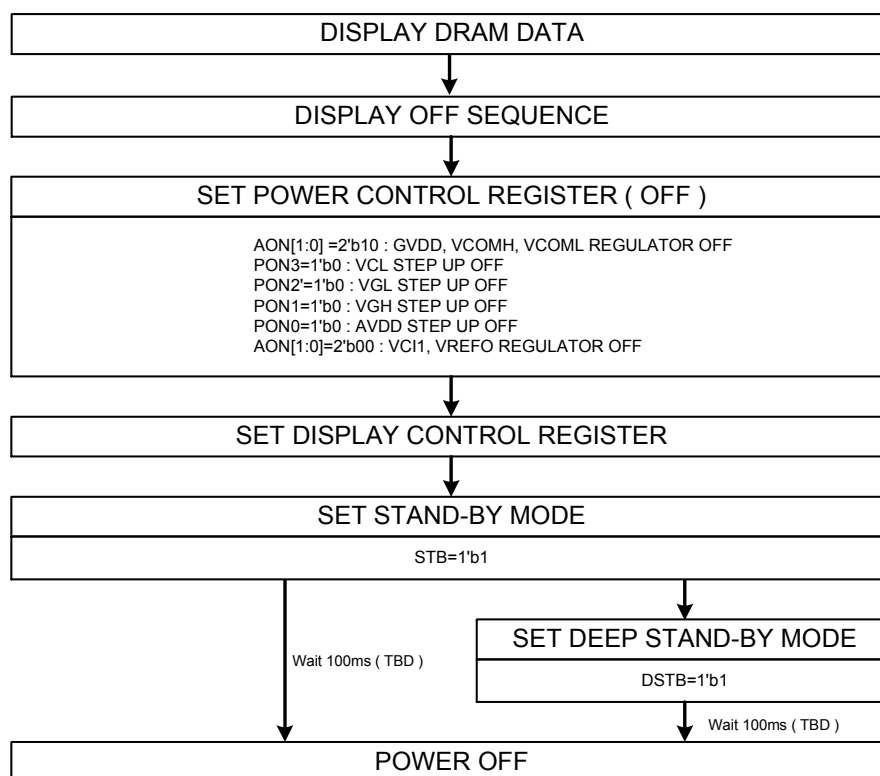


Figure 13-6 : Stand-by In Sequence

13.7. Stand-by Release Sequence

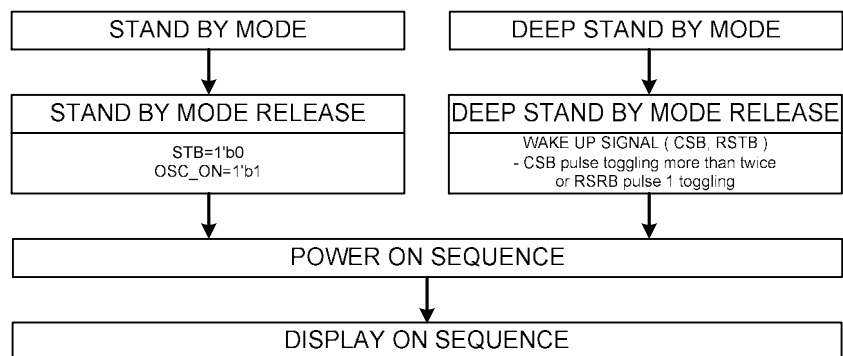
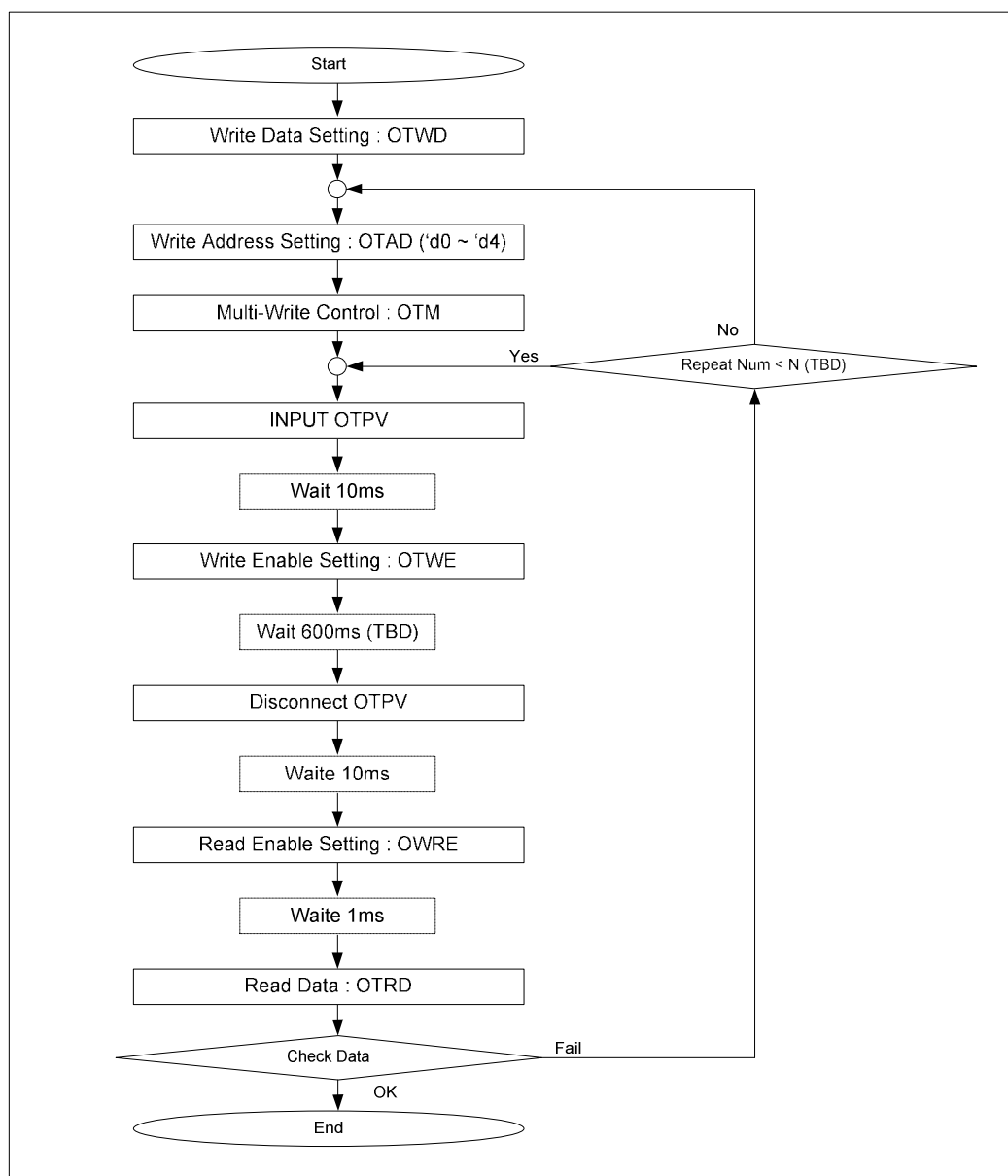


Figure 13-7 : Stand-by Release Sequence

13.8. VCOM Programming Sequence



[NOTE] After programming, the biggest number of address is used for VCOM setting. So, we recommend you should try to set VCOM from low number of address.

Figure 13-8 : NVM program sequence for VCOM adjustment

After programming, the written data into OTP's are loaded to internal actual registers automatically by RSTB assertion, so user need not try to load them intentionally.

14. Electrical Characteristics

14.1. Absolute Maximum Ratings

Item	Symbol	Unit	Rated value	Notes
Power supply voltage (2)	IOVCI – GND	V	-0.3 to +4.6	(1), (2)
Power supply voltage (3)	VCI – GND	V	-0.3 to +4.6	(1), (2), (3)
Power supply voltage (4)	AVDD – GND	V	-0.3 to +6.0	(1), (2)
Power supply voltage (5)	GND – VCL	V	-0.3 to +4.6	(1), (2)
Power supply voltage (6)	AVDD – VCL	V	-0.3 to +9.0	(1)
Power supply voltage (7)	VGH – GND	V	-0.3 to +19.25	(1), (2), (4)
Power supply voltage (8)	GND – VGL	V	-0.3 to +13.25	(1), (2), (4)
Input signal voltage	Vt	V	-0.3 to IOVCI + 0.3	(1)
Operating temperature	Topr	°C	-40 to +85	(1)
Storage temperature	Tstg	°C	-55 to +110	(1)

[NOTE-1] If the LSI is used above the absolute maximum ratings, it might get permanently damaged. Using the LSI within the electrical characteristic limits is strongly recommended for normal operation. If these electrical characteristic limits are exceeded, the LSI will malfunction and cause poor reliability.

[NOTE-2] GND stands for GND and VSSA. GND and VSSA should be equal

[NOTE-3] VCI voltage should have same power voltage

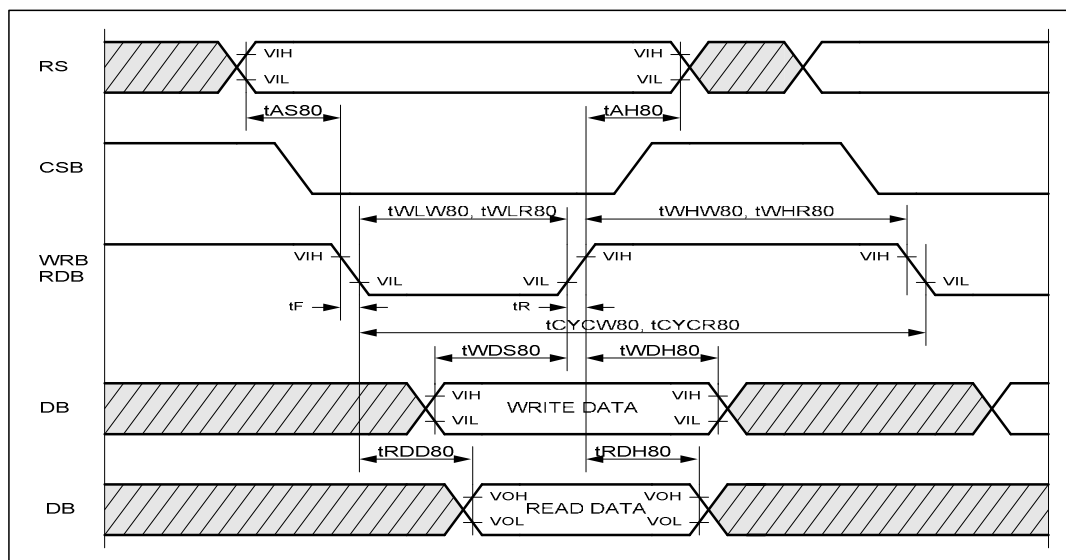
[NOTE-4] Please, keep the maximum gate voltage $|VGH - VGL| \leq 27V$.

14.2. DC Characteristics

Item		Symbol	Unit	Test Condition	Min.	Typ.	Max.
Input high voltage		VIH	V	IOVCI=1.65V to 3.3V	0.8*IOVCI	-	IOVCI
Input low voltage		VIL	V	IOVCI=1.65V to 3.3V	-0.3	-	0.2*IOVCI
Output high voltage (DB[17:0])		VOH	V	IOVCI=1.65V to 3.3V, IOH=-0.1mA	0.8*IOVCI	-	-
Output low voltage (DB[17:0])		VOL	V	IOVCI=1.65V to 3.3V, IOL=0.1mA	-	-	0.2*IOVCI
I/O leakage current		Ili	uA	Vin=0 to IOVCI	-1	-	1
Current consumption (VCI-GND) + (IOVCI-GND)	Normal operation mode	IOP1	mA	Ta=25 degree C TBD	TBD	TBD	TBD
Current consumption (VCI-GND) + (IOVCI-GND)	8-color/32-line partial display mode	IOP2	mA	Ta=25 degree C TBD		TBD	
Current consumption (VCI-GND) + (IOVCI-GND)	Standby mode	ISTB	uA	Ta=25 degree C TBD		TBD	
Step-up output voltage		AVDD	V	Ta=25 degrees C TBD	-	TBD	-
		VGH	V	Ta=25 degrees C TBD	-	TBD	-
		VGL	V	Ta=25 degrees C TBD	-	TBD	-
		VCL	V	Ta=25 degrees C TBD	-	TBD	-

14.3. AC Characteristics

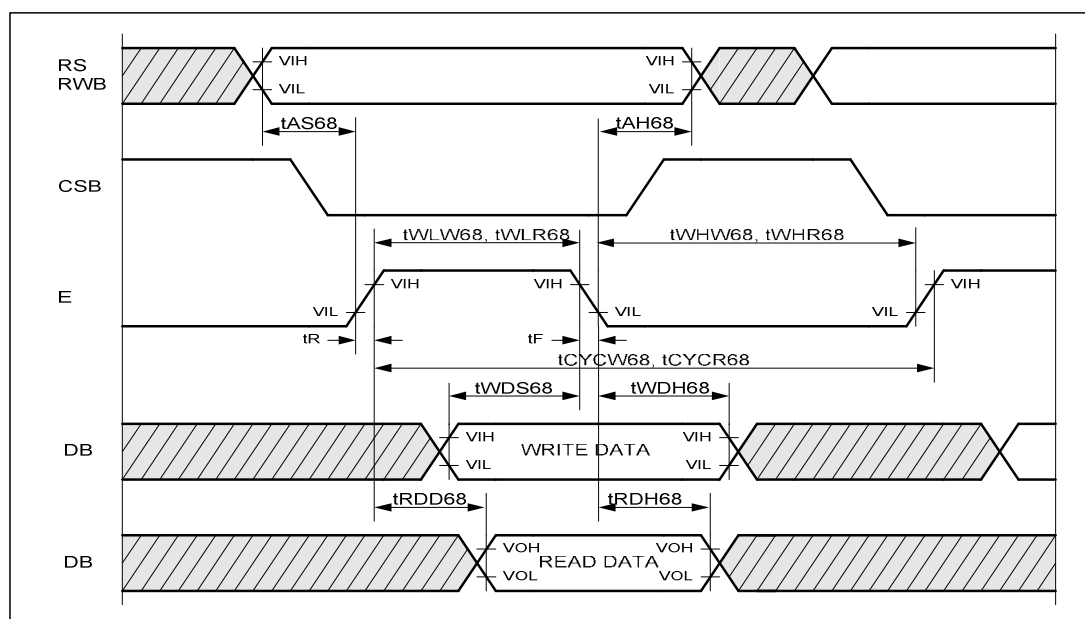
14.3.1. I80-MPU Interface



Parameter	Description	Min	Max	Unit
t_{CYCW80}	Write Cycle Time	50	-	ns
t_{CYCR80}	Read Cycle Time	500	-	ns
t_{WLW80}	Write Pulse Width LOW	20	-	ns
t_{WLR80}	Read Pulse Width LOW	250	-	ns
t_{WHW80}	Write Pulse Width HIGH	20	-	ns
t_{WHR80}	Read Pulse Width HIGH	240	-	ns
t_{AS80}	RS to NCS, NWR Setup Time RS to NCS, NRD Setup Time	0	-	ns
t_{AH80}	RS to NCS, NWR Hold Time RS to NCS, NRD Hold Time	0	-	ns
t_{WDS80}	Write Data Setup Time	15	-	ns
t_{WDH80}	Write Data Hold Time	10	-	ns
t_{RDD80}	Read Data Delay Time	-	200	ns
t_{RDH80}	Read Data Hold Time	5	-	ns
t_R, t_F	Rising/Falling Time (VIH-VIL)	-	5	ns

Figure 14-1 : AC characteristics of I80-system interface

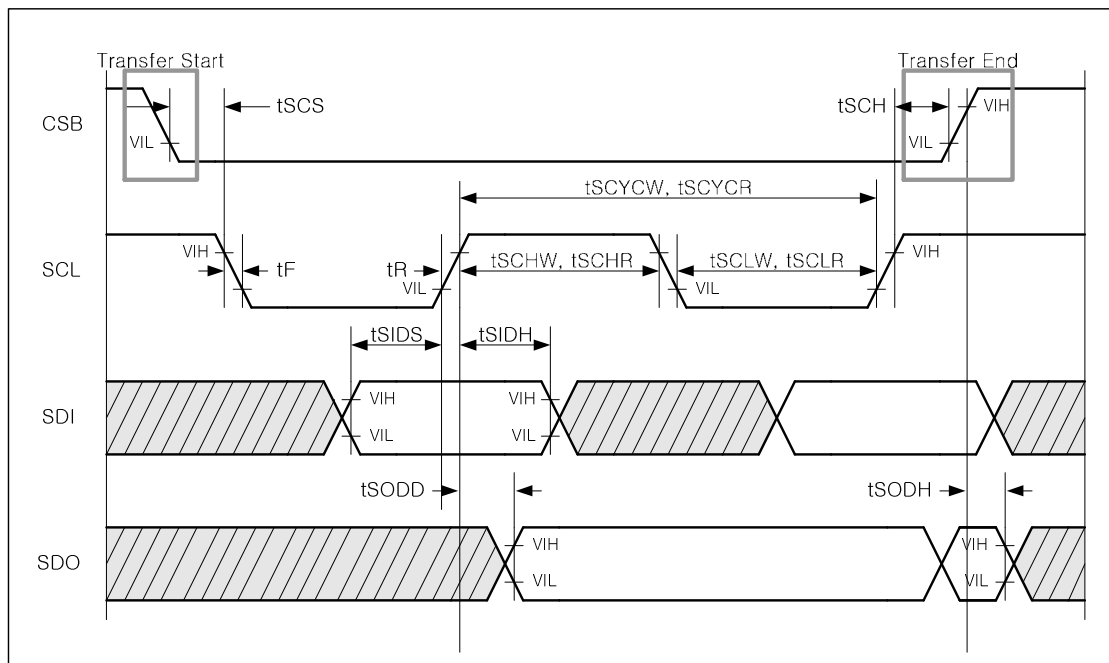
14.3.2. M68-MPU Interface



Parameter	Description	Min	Max	Unit
t_{CYCW68}	Write Cycle Time	50	-	ns
t_{CYCR68}	Read Cycle Time	500	-	ns
t_{WLW68}	Write Pulse Width LOW	20	-	ns
t_{WLR68}	Read Pulse Width LOW	250	-	ns
t_{WHW68}	Write Pulse Width HIGH	20	-	ns
t_{WHR68}	Read Pulse Width HIGH	240	-	ns
t_{AS68}	RS to NCS, NWR Setup Time RS to NCS, NRD Setup Time	0	-	ns
t_{AH68}	RS to NCS, NWR Hold Time RS to NCS, NRD Hold Time	0	-	ns
t_{WDS68}	Write Data Setup Time	15	-	ns
t_{WDH68}	Write Data Hold Time	10	-	ns
t_{RDD68}	Read Data Delay Time	-	200	ns
t_{RDH68}	Read Data Hold Time	5	-	ns
t_R, t_F	Rising/Falling Time (VIH-VIL)	-	5	ns

Figure 14-2 : AC characteristics of M68-system interface

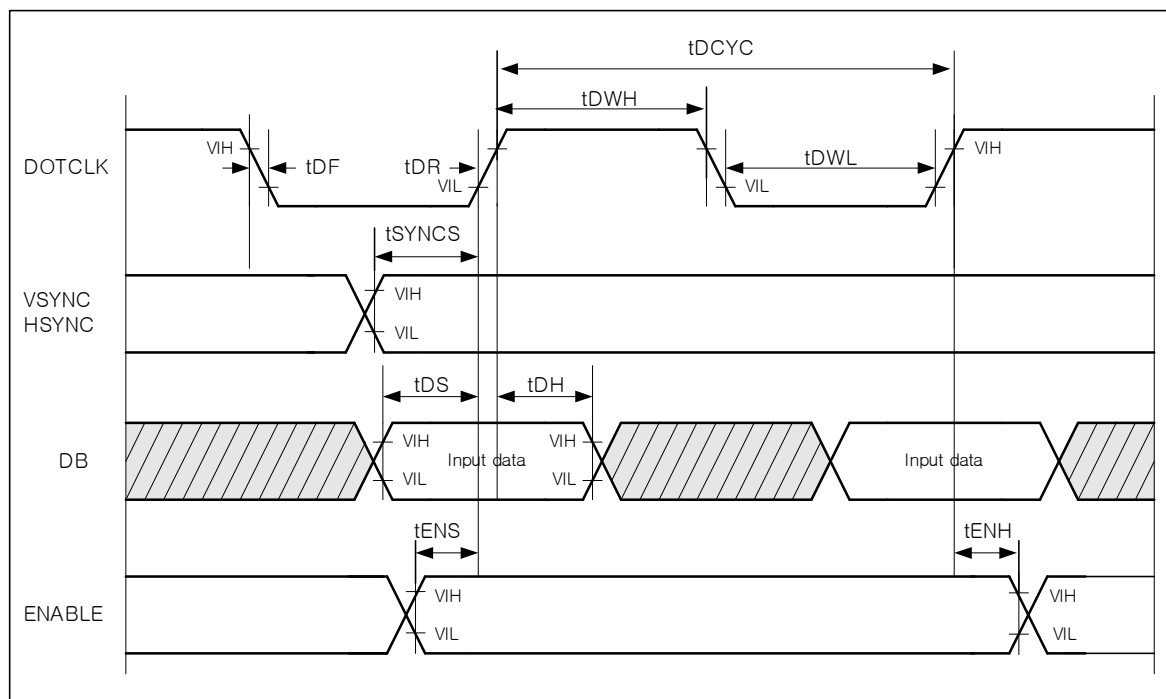
14.3.3. Serial Peripheral Interface (SPI)



Parameter	Description	Min	Max	Unit
tSCYCW	Serial Clock Write Cycle	100	-	ns
tSCYCR	Serial Clock Read Cycle	500	-	ns
tSCHW	Pulse Width High for Write	40	-	ns
tSCHR	Pulse Width High for Read	250	-	ns
tSCLW	Pulse Width Low for Write	50	-	ns
tSCLR	Pulse Width Low for Read	240	-	ns
tSCS	CSB Setup Time	20	-	ns
tSCH	CSB Hold Time	60	-	ns
tSIDS	SDI Setup Time	40	-	ns
tSIDH	SDI Hold Time	30	-	ns
tSODD	SO Delay Time	-	130	ns
tSODH	SO Hold Time	5	-	ns
tR, tF	Rising/Falling Time (VIH-VIL)	-	5	ns

Figure 14-3 : AC characteristics of SPI

14.3.4. RGB Interface



Parameter	Description	Min	Max	Unit
t_{DCYC}	DOTCLK period	50		ns
t_{DWL}	DOTCLK pulse width low	20		ns
t_{DWH}	DOTCLK pulse width high	20		ns
t_{DR}/t_{DF}	DOTCLK rising/falling time		5	ns
t_{SYNCS}	VSYNC,HSYNC setup time	30		ns
t_{ENS}	ENABLE setup time	20		ns
t_{ENH}	ENABLE hold time	20	35	ns
t_{DS}	Input data setup time	30		ns
t_{DH}	Input data hold time	20		ns

Figure 14-4 : AC characteristics of RGB Interface

14.3.5. LCD Output Driving Capability

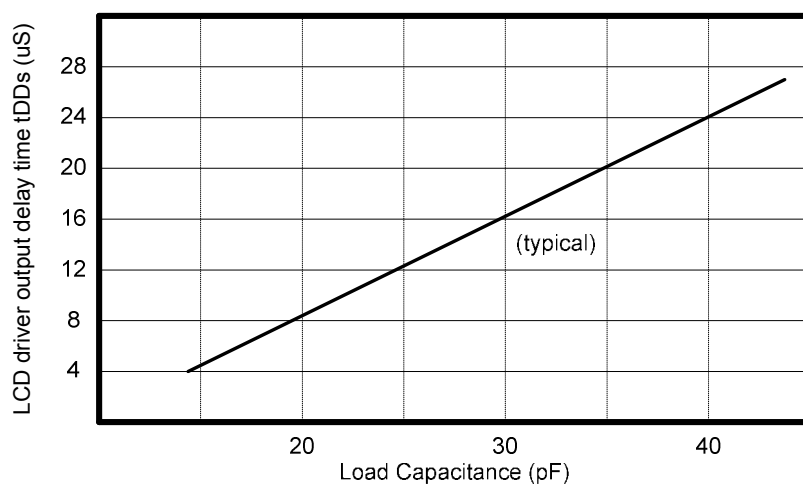


Figure 14-5 : Source Driver Output Delay Time (R = 10K ohm)

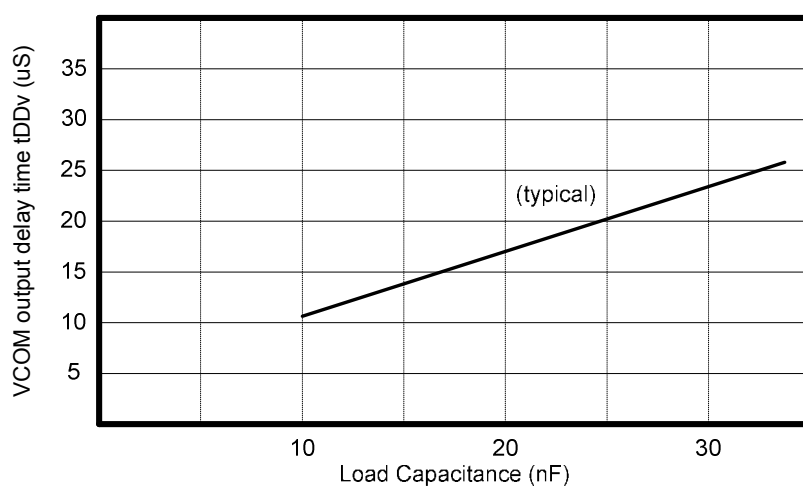


Figure 14-6 : VCOM Output Delay Time (R = 100 ohm)

Appendix

A. Backlight Control

TA7601 supports two kinds of backlight control scheme. One is external manual control and the other is display data adapted control with display data processing.

A. 1. Backlight Control Flow

Figure A-1 shows backlight control flow. TA7601 generates a PWM signal and backlight is controlled by the PWM signal. Backlight ON/OFF is controlled by BLC_ON register. There are two kinds of backlight control scheme using SMLC_ON register.

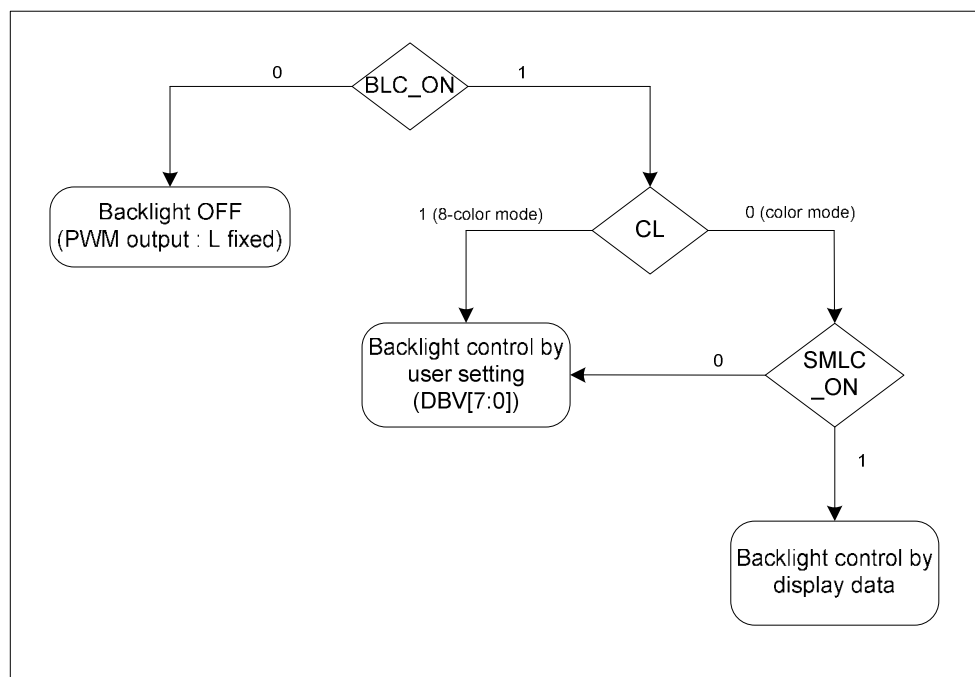


Figure A-1 : Backlight Control Flow

SMLC_ON = "L" : A PWM signal for backlight control is generated by DBV[7:0] value. At this time, display data is not manipulated.

SMLC_ON = "H" : A PWM signal for backlight control is generated by display data adaptively. At this time, brightness of display data are enhanced by SMLC (Smart Mobile Luminance Control) algorithm.

In detail, a PWM signal is generated using both SMLC_DBV[7:0]. SMLC_DBV[7:0] value is selected by SMLC algorithm among

LVx_DBV[7:0] registers.

The original brightness of display data is defined as 8-level brightness by SMLC algorithm. As a result of brightness level, the amount of brightness enhancement is decided. User can check brightness level of display data as reading SMLC_IMG_BR_LEVEL[7:0] registers.

[NOTE] Backlight brightness means PWM resolution and range is from 'd0 to 'd255.

So, Backlight brightness could be adjusted delicately.

A. 2. SMLC Algorithm

The original brightness of display data is defined as 8-level using histogram analysis. The amount of brightness enhancement is different according to the brightness level of original image.

TA7601 supports two kinds of enhancement mode. The difference of two enhancement modes is the amount of brightness enhancement. One is less enhancement (less power reduction) and better image quality. The other is more enhancement (more power reduction) and worse image quality. User could select SMLC mode using SMLC_MODE register.

SMLC_MODE = "L" : lower power reduction and better image quality.

"H" : higher power reduction and permitted a little image distortion

SMLC_IMG_BR_LEVEL[7:0] shows the brightness level of display data.

Table A-1 : Brightness level of display data

SMLC_IMG_BR_LEVEL[7:0]	The Brightness level of display data
8'b10000000	8-level (bright)
8'b01000000	7-level
---	---
8'b00000010	2-level
8'b00000001	1-level (dark)

The above table shows reference value of backlight brightness.

This value should be adjusted by the characteristics of panel and white LED driver IC.

Table A-2 : Backlight brightness according to the image brightness level

Image brightness level	SMLC_DBV[7:0] @SMLC_MODE is "High"	SMLC_DBV[7:0] @SMLC_MODE is "Low"	Register (LVx_DBV[7:0])
1	'd145	'd165	LV1_DBV
2	'd153	'd165	LV2_DBV
3	'd155	'd175	LV3_DBV
4	'd170	'd175	LV4_DBV
5	'd170	'd198	LV5_DBV
6	'd193	'd198	LV6_DBV
7	'd216	'd216	LV7_DBV
8	'd255	'd255	LV8_DBV

A. 3. PWM Signal and Dimming Function

The PWM signal is generated by DBV or SMLC_DBV.

Frequency range of a PWM signal is about 520Hz ~ 20KHz depending on OFC register or DOTCLK frequency. The clock source for PWM generation is internal oscillator (DM=2'b00 or 2'b10) or divided DOTCLK (DM=2'b01) (For detail, refer to the table 7-16 : Clock cycles per horizontal line).

The frequency below 100Hz is likely to cause visible flicker in the light emitted by the LED.

Figure A-2 shows an example of waveform.

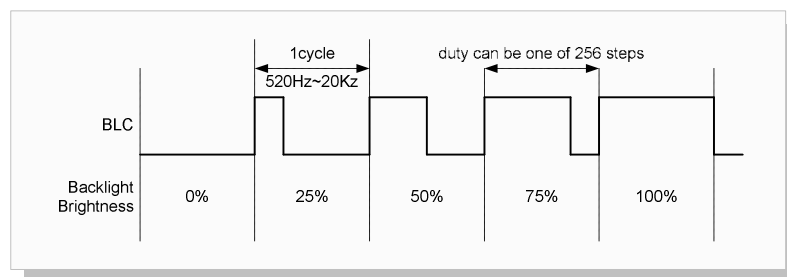


Figure A-2 : Period of PWM signal

TA7601 supports dimming function of the PWM signal using DIM and TR[1:0] registers.

The PWM pulse width is changed slowly when DBV or SMLC_DBV is changed.

Transition time is controlled by TR[1:0] registers.

Figure A-3 shows conceptual operation of dimming function.

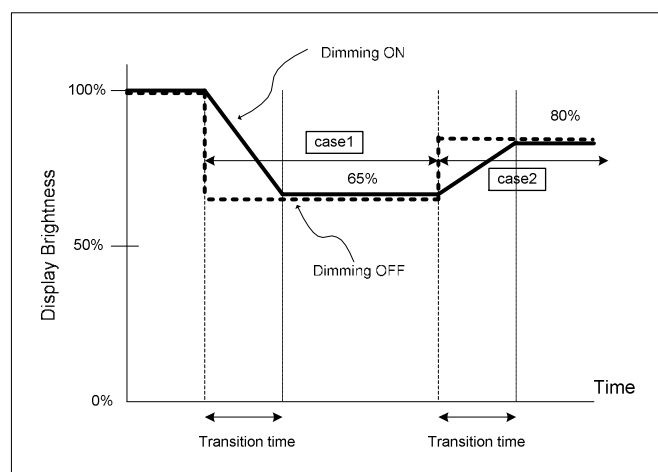


Figure A-3 : Dimming Function

B. Application Diagram

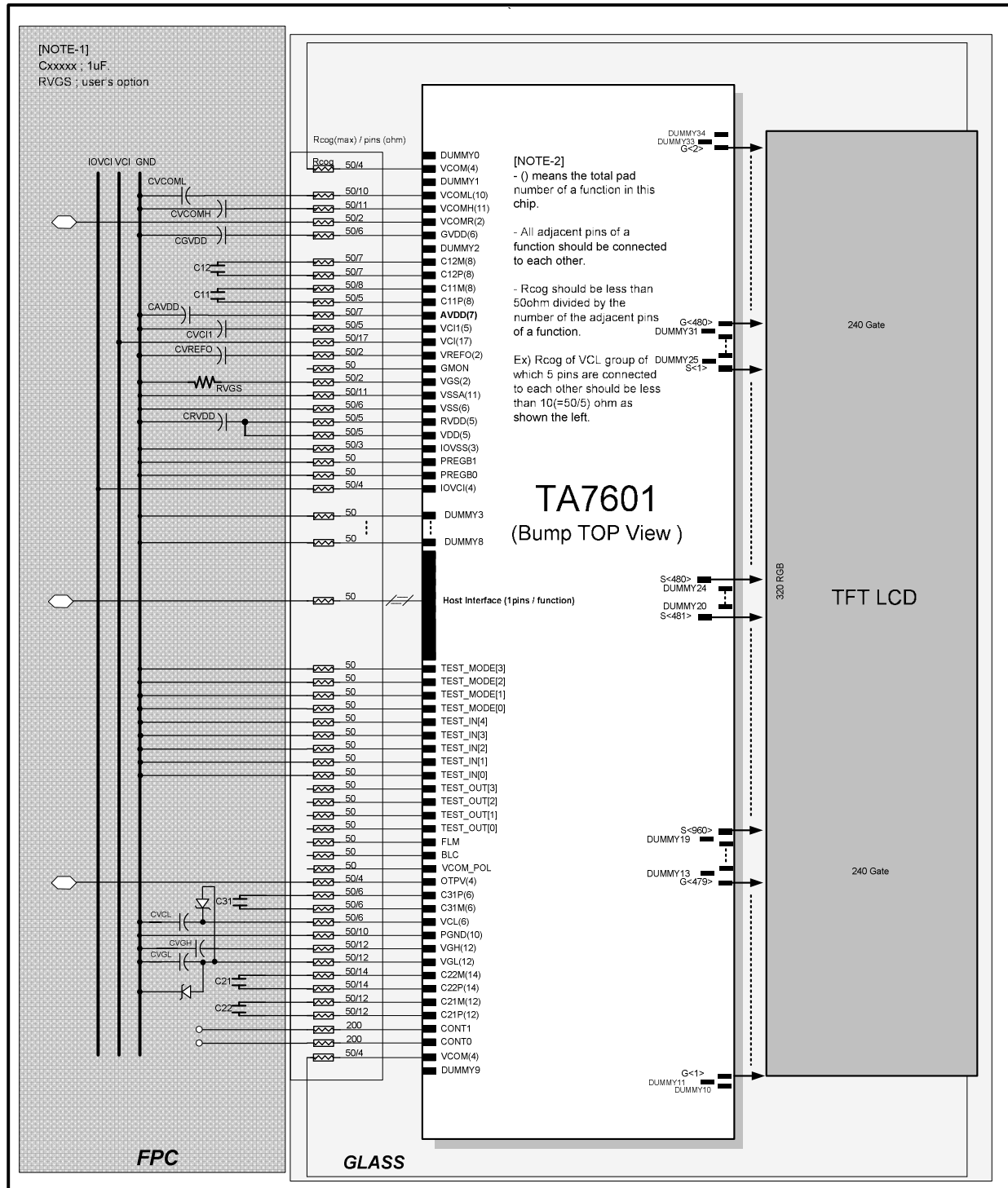
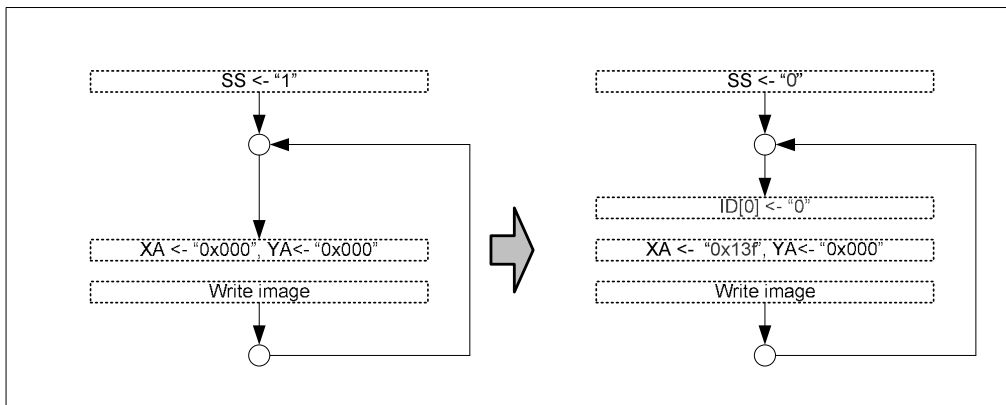


Figure B-1 : Application Diagram of TA7601

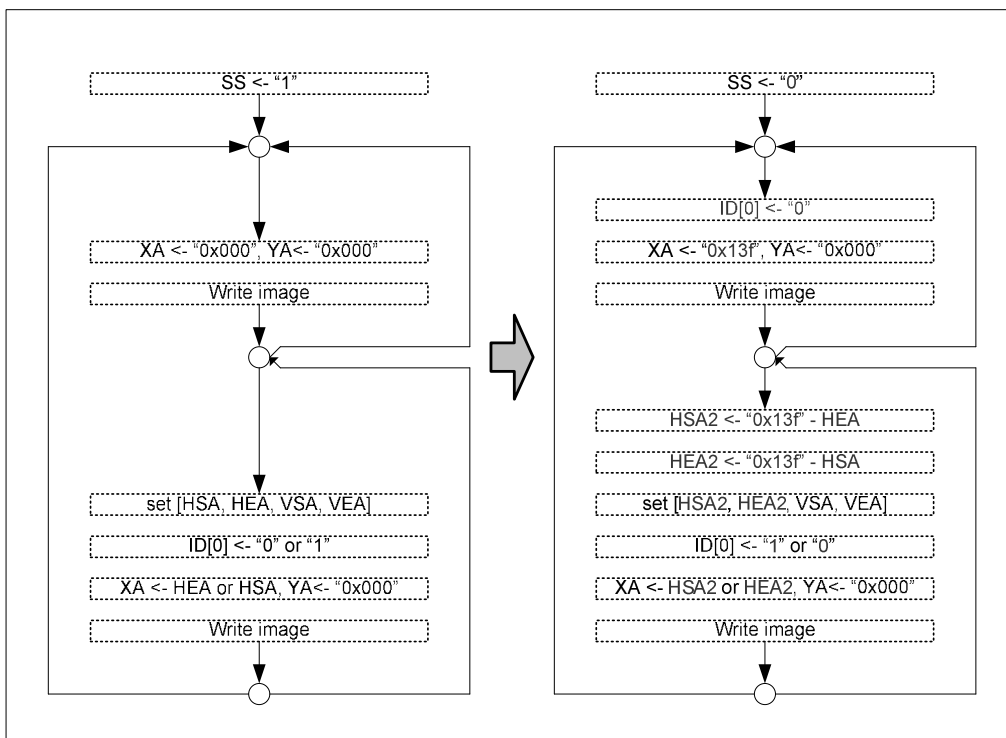
C. Using ID[0] instead of SS to change source output direction

When you use ID[0] instead of SS to change source output direction, you'd better follow the sequence as below for some cases.
If you do not want to change source output direction(; SS=0), you don't have to read this chapter.

C. 1. Changing source output direction without windowed area



C. 2. Changing source output direction with windowed area



Revision History

Ver #	Modified Items	Page	Remark
0.0	Preliminarily released		2008.1.15
0.1	64 potentiometer → 247(max) potentiometer	12	2008.1.24
	Output Bump Rule changed	16	2008.1.24
	Pad coordinates are added.	18	2008.1.23
	Pin Assignment is added.	30	2008.1.24
	Instruction Table is changed.	42	2008.1.24
	BLC_MIX register is added	55	2008.1.24
	PWM Frequency is updated.	58	2008.1.24
	BLC_MIX_MIN register is added	75	2008.1.24
	CPU_IF data setup/hold timing parameter is changed	161, 162	2008.1.24
	RGB_IF ENABLE timing parameter is changed	164	2008.1.24
	Application Diagram is added.	170	2008.1.23
0.2	Description of DUMMY3~DUMMY8 is modified	37,	2008.1.29
	PWM waveform is changed.	56, 169	2008.1.26
0.3	Description of OTP usage is updated.	92	2008.02.28
	PREGB[0] should be tied to “high”	37	2008.04.16
	VCOM Programming Flow is modified(OTPV)	157	2008.05.02
0.4	Progressive scan mode → Sequential scan mode	47	2008.06.20
	Interlaced scan mode → Alternate scan mode	47	2008.06.20
	CSB condition for inactivation is modified	33	2008.06.23
	TP_PASS is described.	43, 93	2008.07.17
0.5	SS description is removed.	47	2008.08.06
	ID description is detailed	51	2008.08.06
	Appendix.C is added	170	2008.08.06
0.6	SS is removed	45	2008.08.21
	“(R67h)” is added	92	2008.08.21

[NOTE] Ver0.xx means that the document is preliminary version. So content of it is design target and is not fixed yet.

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